

A Two stage stand alone Solar PV system

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Under the guidance of

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&

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DEPARTMENT OF ELECTRICAL ENGINEERING

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MAY, 2016



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CERTIFICATE

This is to certify that the project entitled "**Two Stage Stand Alone Solar PV System**" submitted by Peddiraju Vamsi Krishna (214EE4258) in partial fulfilment of the requirements for the award of Master of Technology degree in Power Electronics and Drives, Department of Electrical Engineering at National Institute of Technology, Rourkela is an authentic work carried out by him under my supervision and guidance.

To the best of my knowledge, the matter embodied in this thesis has not been submitted to any other university/Institute for the award of any Degree.

Place:

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Date:

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Abstract

Stand-alone systems based on solar photovoltaic (PV) have developed as a sustainable alternative pertaining to issue of electrification in areas particularly where the grid is not present. Main challenges in scheming this kind of systems are

- 1) Maximum power extraction from PV array
- 2) Dc to ac conversion
- 3) Protecting battery from over discharging and overcharging and
- 4) Facilitating satisfactory stepping up of voltage.

As many objectives are needed to be met, schemes hitherto for standalone systems need a minimum of three converter stages, resulting in significant decline in efficiency and reliability of system. To tackle this problem, a two stage stand-alone topology comprising a novel transformer coupled dual input converter (TCDIC) is connected to a normal full bridge inverter is discussed in this thesis. Discussed TCDIC can facilitate charge control of battery while tracking maximum power point and keeping proper voltage level at load terminal. Mathematical model of TCDIC through small signal based approach is also included. A suitable control strategy for TCDIC is also presented to generate pulses. The operational efficiency of this topology is verified by performing simulation studies in detail.

Key Terms: solar photovoltaic (PV) converter, stand-alone PV system, Battery charge security, dual input dc to dc converter.

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List of Abbreviations

Abbreviations	Description
MPP	Maximum power point
MPPT	Maximum power point tracking
TCDIC	Transformer coupled dual input converter
RESs	Renewable energy sources
PV	Photovoltaic
STCs	Standard test conditions
I_{mpp}	Panel Current at mpp
V_{mpp}	Panel voltage at mpp
V_{pv}	Panel voltage
V_b	Battery voltage
V_{dc}	DC link voltage
I_{pv}	Panel current
I_b	Battery current
i_L	Inductor current
C_p	Polarization capacitor
C_{10}	Nominal capacity (in ampere-hours) after a 10-h charging
I_{10}	Charge current corresponding to C_{10} .
V_{cb}	Electromotive force (in volts)

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Chapter 1

INTRODUCTION

1.1. Overview

The Domestic loads in India normally need a voltage of 230-V and a frequency of 50-Hz single phase supply. As the output power from battery and PV array is in form of dc, dc to ac inverter is needed for supplying load. To produce an alternating voltage of 230 V for these applications, full bridge inverters of single phase are normally used that are needed to maintain a dc voltage of magnitude of 350 V or even excess. By connecting many batteries and/or PV modules in series the necessity of high input dc link voltage for inverter can be met. But, PV systems connected serially leads to some amount of decrease in output of power when subjected to non-uniform irradiance values. To tackle the present problem, either an additional converter(s) or intricate algorithm of maximum power point (MPP) tracking (MPPT) is needed. The several standard 12-V batteries serial connection results in an increase in size and cost of the system. Further, the application of a high level voltage for battery and/or PV array asks a demanded design for system to stand by to the wellbeing of equipment along with personnel.

According above mentioned restrictions, systems based on stand-alone schemes are normally designed with voltage ranges of low value for battery and the PV array in ambit of 24 to 36 V. But, this leads to the necessity of a voltage gain of high value for complete system to ascertain a 230-V ac supply at end where load is placed. Such gain of high value can be obtained by incorporating step-up transformer of low frequency on output of inverter. But, this will lead to increase in volume, burden and size of the system. To tackle such hurdle, necessity of high gain can be obtained by intermediary converters (dc to dc) which interface battery and PV to dc link of inverter. Such thing can be accomplished by incorporating three stages of dc to dc conversion. But, as the increase in number of converters go up there will be decrease in efficiency and causes system reliability to decrease. Multi winding transformer of high gain based converters can be put in use for tackling such problem. But, such systems need controlled switches eight in number as minimal requirement besides switches four in number which are needed to actualize inverter. moreover, present stand alone systems incorporate an extra consecrated converter (dc to dc) to actualize operation at maximum power point. We know that PV power is procurable for only some part of day, utilization of such above mentioned converter will not be satisfactory. A system in which use of a consecrated dc to dc converter for operation at maximum power point is evited is discussed in [12]. Such topology is having battery and PV array connected in series and is designed for specific purposes like lighting system feeding by PV. But, such topology is having these restrictions: 1) Resonant elements

presence results in system sensitive to parametric quantities variations; 2) Allowable ambit in switch's duty cycles is also restricted to sealed ambit; and 3) Gain in voltage is also restricted. But, the above mentioned topologies have to bypass PV array by an inductor and a diode when PV power reaches zero, which leads to gain reduction effectively as battery and PV are series connected. To tackle these restrictions found in [12], a transformer coupled dual-input converter (TCDIC) based stand-alone system is discussed my thesis. The input side of TCDIC is accomplished by connecting battery and PV array in series, thereby easing converter ability to boost. Voltage level of TCDIC on output side is farther increased by integrating step up transformer of high frequency. Unparalled characteristic of TCDIC is that its ability to perform voltage boosting, charge control of battery and MPPT operation through utilising a proper logical algorithm of control. so, all features which are obtainable in the existing standalone systems by incorporating two or more stages of dc to dc converters can be attained by TCDIC which is of single stage. Conventional full bridge inverter is connected on output side of TCDIC to attain dc to ac conversion. Introductory doctrine of present topology and its rudimentary analysis is presented in [11], and afterwards, farther work that was done on this topology is presented [10]. Elaborated analysis of TCDIC, its operation, mathematical modelling, control structure and simulated performance are discussed in chapter 3.

1.2. Literature Review

A Comprehensive approach to Modelling of Photovoltaic Arrays is presented in [1], which discusses the aspects of pv cell i.e., its structure, its operating principle, output variations with respect to irradiance and temperature, Modelling of pv devices, arrays and also gives detailed explanation about how to improve the model. There are so many ways of designing or realising pv cells such as single diode model, diode model with two diodes, diode model with three diodes which are discussed in [2]-[4], thereby increasing the number of diodes represent the effects not described by lesser number of diodes model(As effect of carriers recombination). As a conclusion we can infer single diode model is best suited for power electronic applications for its simplicity without compromising accuracy.

In designing pv cells, there are so many parameters which are to be taken into consideration. In the process of realising the model, it leads to more complications. In [5], the assumptions which are to be taken to simplify the model has been presented. After designing the pv array and while in operation, tracking maximum power point is another challenging task, which can be tracked through various maximum power point tracking algorithms, out of which P&O (perturb & Observation) presented in [6] is most widely used, simple in designing and less number of sensors used.

The other methods through which maximum power can be tracked are presented in [7]. Few of them are more complex in implementing when compared to perturb and observation

algorithm and they require more sensors than that which leads to less economic benefit. Experimental demonstration of seven majorly used MPPT algorithms in [8]-[9] gives us a clear understanding of which method to be adopted according to the application such as whether we have to compromise on lucidity front or accuracy front. If we are more concerned with lucidity and less bothered about ripple in voltage, we can go for P&O scheme, if vice versa then IC scheme is to be preferred, The topology which is used in this work is taken from [10], is a new topology incorporating both pv panel and battery in two different stages to inverter through coupling transformer to supply a load in remote areas. The reference illustrates the basic topology, operating principle, advantages, small signal based analysis, control structure of that topology.

The basic concept behind the earlier mentioned reference is presented in [11], its optimised version and detailed analysis is presented in earlier reference. This so called two stage topology has been evolved after noting the limitations in single stage topology presented in [12], such as resonance elements in circuit leads to parameter variations in the system, duty ratio and voltage gain limited. The TCDIC mathematical model through small signal based analysis is used to design controllers for the closed-loop operations is presented in [13]. The battery used in the two stage topology is to be operated such that it should not be over charged or over discharged for the battery life time to be longer, and to always maintain its state of charge in moderate level. The algorithm for this is described in [14] through a simple modelling of the battery through a resistor-capacitor model and its analysis leading to a flowchart to be followed to meet our objectives.

1.3. Motivation

Electricity is considered as a necessity for holy existence of mankind. The socio and economic development of a country is strongly dependent on the level of usage of electrical energy. In the current scenario where India is consuming much less when compared to many emerging economies. By bad luck, nearly 30 crore citizens of India have no facility to electricity, where major portion of mentioned figure live in remote places. To ameliorate this situation of scarcity of electrical energy, many initiatives were taken such as rural electrification at brisk pace and the many of them are concentrated towards the renewable energy sources (RESs) to generate electricity which is advantageous in many ways. From many years, one of the most sustainable alternative among the existing RESs is solar photovoltaic (PV). But, the existence of power from PV is sporadic with respect to time, and so, standalone systems based on PV requires a storage device to store energy which is normally done by employing bank of batteries. Moreover, such systems also need integration of power electronic converters to form an interface among load, the battery, and the PV array. Main work of my project is performing simulation of reliable and efficient interface through power electronics for a stand-alone system based on PV. The interface is designed for providing to condition of loading in India but can be broadened to other conditions of loading also with suited alterations of the parametric quantities of design.

1.4. Objectives

The main objectives of my work are

1. Modelling of Photo voltaic array
2. Extraction of maximum power from PV array
3. Protection of battery from over discharging and overcharging
4. Conversion from dc to ac
5. Provision for adequate voltage boosting.

1.5. Thesis Organization

This thesis is organized into six chapters. For the reader to have a strong and complete understanding of the work done, it has been presented in a lucid and sequential way. The content inside the thesis will be briefed now.

Chapter 1 encompasses the introduction into the main work i.e., overview or the basic task of the work and motivation behind choosing this project, literature survey done to proceed into the work and objectives to be met for the work to fructify.

Chapter 2 presents modelling of PV arrays, their operating principle, improving the already designed models, their characteristics, basic equations involved in modelling, output variations when subjected to parameter changes namely temperature and insolation, concept of maximum power point tracking, different methods of tracking maximum power point, simplest and economical among other methods, algorithms to implement.

Chapter 3 deals about the TCDIC (Transformer coupled dual-input converter), the topology which is used in the main circuit to supply loads in the remote areas, this chapter comprises operating principle of this topology and its modes of operation, advantages and limitations of this topology when compared to other topologies, mathematical model through small signal based analysis and control strategy to generate pulses to the switches.

Chapter 4 presents Battery current tracking algorithm which is required to maintain battery in moderate state of charge condition to prevent from over discharge. This algorithm also generates maximum input battery current with respect to state of charge to prevent battery from over charging phenomenon thereby resulting in longevity of battery life time.

Chapter 5 consists of Results and Discussions of simulation performed of the main stand alone system. The simulation results show steady state and transient responses of various parameters such as panel voltage, panel current, battery current, DC link voltage, Load voltage. Also demonstrates various modes of operations of the circuit and transition of modes while in operation

Chapter 6 which is last chapter of the thesis is comprises of Conclusions of the present work i.e., whether the objectives have been met or not and Scope for the future work on this topology: Regarding grid integration of stand alone pv system through this topology.

Chapter 2

Modelling of Photo voltaic array and Extraction of maximum power

2.1. Operation of a PV cell

A photo voltaic cell is normally a diode made of semiconductor where its $p-n$ junction is displayed to sun light. These Photovoltaic cells are manufactured with many classes of semiconductors employing various manufacturing processes. In present times and particularly in commercial fields only poly crystalline and monocrystalline silicon cells are found. These Silicon PV cells are affiliated to electric ends through a thin layer of bulk Si or a thin Si film. For forming the $p-n$ junction, one side of Si layer has to be doped. A thin metallic grid is fixed on Sun facing side of semiconductor. Fig. 1 approximately shows PV cell's physical structure.

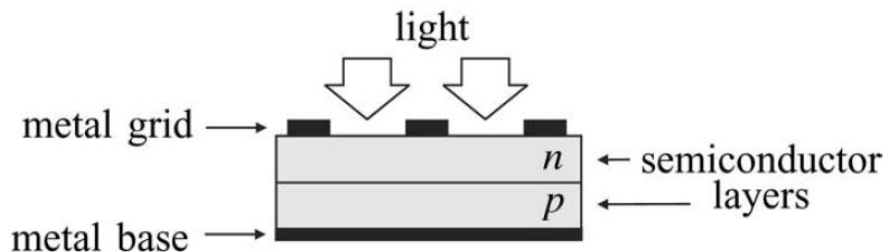


Fig. 1. Physical structure of a PV cell.

charge carriers are generated when sun light falls on the cell that lead to electric current provided cell was in short circuited condition. Generates charges only when photon energy which incidents is satisfactorily enough to detach the covalent electrons of semiconductor. Such process is dependent on wavelength of incident light and the material with which semiconductor is made. Normally, the PV concept is elaborated as absorption of irradiance from sun, transport and generation of carriers which are free at $p-n$ junction, and collection of such electric charges at ends of PV cell. Rate at which these electric carriers generates depends on the ability of absorption of that particular semiconductor and incident light's flux. Ability to absorb is majorly dependent on bandgap of semiconductor, on reflectance of cell surface (which is dependent on treatment of shape and surface), on intrinsic concentration of carriers of semiconductor, on rate of recombination, on mobility of electrons, on temperature subjected, and on many alternate reasons. Irradiance of on rate of recombination is comprised of photons with dissimilar energies. Photons which have energies less than bandgap of PV cell are fruitful and generates zero electric current or voltage. Photons with energy higher when compared to bandgap generates electric current, but only energy related with bandgap is usable, remaining energy is dispelled as heat in PV cell's body. Lower bandgapped Semiconductors may take reward or a major portion of spectrum of radiation, but generated voltage is low. Silicon is not only one, and perhaps not best indeed, semiconductor material to make PV cells, however this is one and only unique

one whose manufacturing process is very much economical in large scale. Materials other than this can give better efficiency in conversion, but at impractical costs.

2.2. Modelling of PV Devices

2.2.1. Single Diode model of a PV Cell

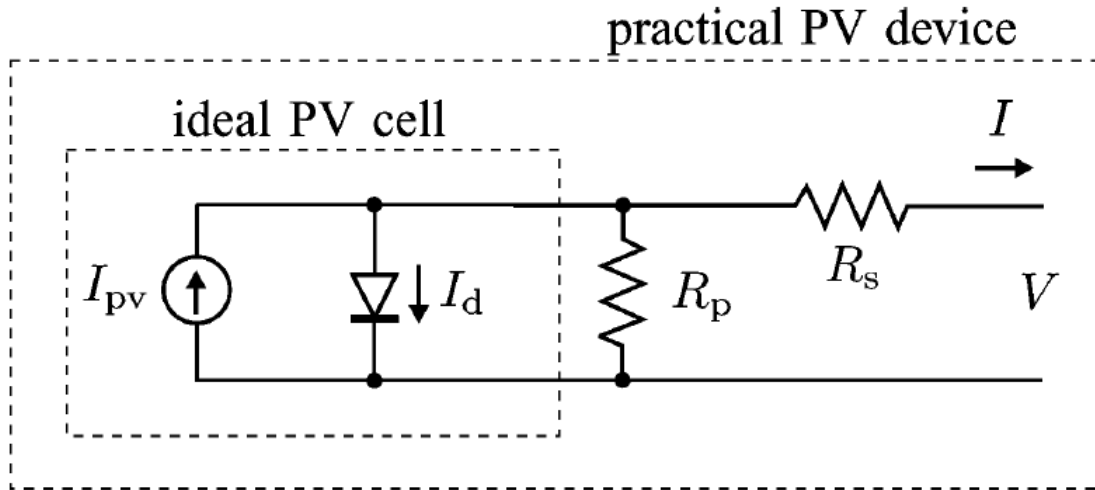


Fig. 2. Single diode model of the conventional PV cell and its tantamount circuit of a practical PV device taking its parallel and series resistances into the account.

Fig. 2 shows ideal PV cell's tantamount circuit diagram. Rudimentary equation from semiconductors theory which mathematically illustrates I–V characteristics of PV cell in ideal way is

$$I = I_{pv, cell} - I_{0, cell} \left[\exp \left(\frac{qV}{akT} \right) - 1 \right] \text{-----(1)}$$

$$I_d = I_{0, cell} \left[\exp \left(\frac{qV}{akT} \right) - 1 \right] \text{-----(2)}$$

Where

$I_{pv, cell}$ is generated current when sunlight is fallen(it is directly relative to insolation)

I_d is Shockley diode equation

$I_{0, cell}$ is leakage or reverse saturation current through diode

q is charge of an electron ($1.60217646 \times 10^{-19}$ C)

k is Boltzmann constant ($1.3806503 \times 10^{-23}$ J/K)

T (in Kelvin) is p–n junction's temperature

a is the diode ideality constant.

Fig. 3 displays I–V Characteristics of typical PV cell obtained from (1).

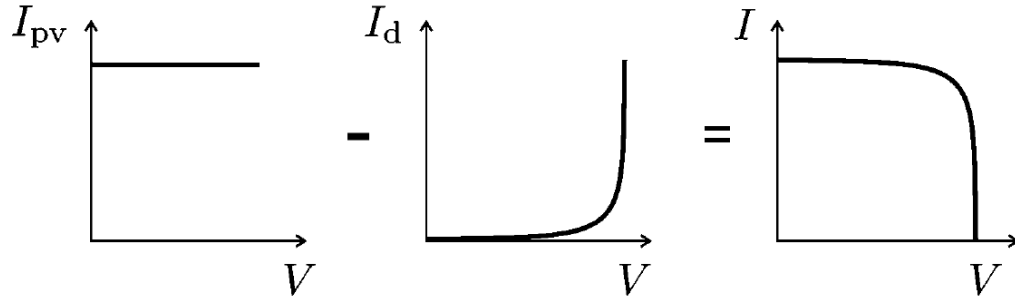


Fig. 3. I–V Characteristics curve of the PV cell. The total cell current I is combination of the the diode current I_d and light-generated current I_{pv} .

2.2.2. Modelling the PV Array

The rudimentary equation of primary PV cell does not take I–V characteristics of pragmatic PV cell into consideration. Pragmatic arrays are comprised of many PV cells connected and noticing of characteristics of those at ends of PV array makes inclusion of extra parametric quantities to rudimentary equation imperative.

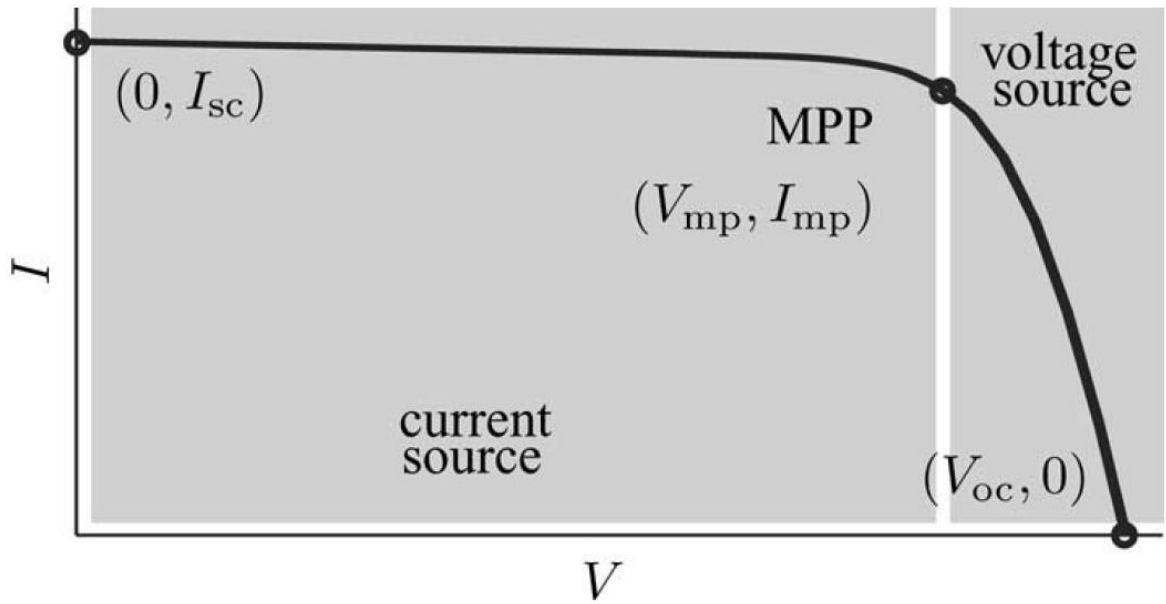


Fig. 4. I–V Characteristics curve of a practical PV device and three remarkable points: open circuit (V_{oc} , 0), MPP (V_{mp} , I_{mp}) and short circuit (0, I_{sc}).

$$I = I_{pv} - I_0 \left[\exp \left(\frac{V + R_s I}{V_t a} \right) - 1 \right] - \frac{V + R_s I}{R_p} \quad (3)$$

where I_0 , I_{pv} are saturation, photovoltaic (PV) currents respectively

$V_t = \frac{N_s k T}{q}$ is array's thermal voltage

R_p is tantamount parallel resistance

R_s is tantamount series resistance of array

N_s is number of cells connected in series.

parallel connected cells enhances value of current and series connected cells facilitate higher voltages at output. If array comprises N_p cells in parallel connection saturation and PV currents can be conveyed as $I_0 = I_0, \text{ cell } N_p$, $I_{pv} = I_{pv, \text{ cell } N_p}$. This (3) develops I–V curve in Fig. 4, in which three main points are marked: open circuit ($V_{oc}, 0$), MPP (V_{mp}, I_{mp}) and short circuit ($0, I_{sc}$).

Equation (3) depicts single diode model shown in Fig. 2. There are many more advanced models which give better exactness and suit for different applications. An extra diode is incorporated to bring in effect of carriers recombination effect into consideration. Diode model in which three diodes are taken is also there which incorporates other phenomena which is vomited in earlier models. Preferring lucidity, single diode model shown in Fig. will be discussed here. Such model extends better compromise between lucidity and exactness, and is widely used, many a times with reductions but eternally with fundamental structure comprised of a parallel connection of diode and current source. Lucidity of single diode model providing way for modifying parametric variations and enhancements make this model apt for designers to make a simple model for PV based power electronic circuits simulation.

PV arrays Manufacturers, rather than I–V equation, specify only some experimental data about thermal and electrical characteristics of these arrays. But, the parameters which are needed to be modified or adjusted for improving the model will not be specified in the data sheets of that product such as semiconductor's bandgap energy, diode ideality constant, reverse saturation current of diode, shunt and series resistances, PV current. Generally many PV array datasheets specify the following data: peak output power ($P_{max,e}$) which is determined experimentally, temperature coefficient/short circuit current (K_I), open circuit voltage/temperature coefficient (K_v), current at MPP (I_{mp}), short circuit current under nominal conditions ($I_{sc,n}$), voltage at the MPP (V_{mp}), open circuit voltage under nominal conditions ($V_{oc,n}$). This data is constantly given according to the standard test conditions (STCs) or nominal conditions of solar insolation and temperature. Few manufacturers specify I–V curves for different temperature and insolation levels. These curves make modification and substantiation of wanted mathematical I–V equation easier. Fundamentally, anyone can access this data from of PV array's datasheet.

Electric generators will normally be categorised into sources of voltage or current. Pragmatic PV array gives a hybrid behaviour, that is of voltage or current source dependent on operating point which is displayed in Fig. 4. Pragmatic PV device will have resistance

in series, R_s where its affect is heavier while device operation is under voltage source region and parallel resistance R_p has much affect when operation is under current source region. Resistance R_s is addition of device structural resistances. Fig. 1 depicts structure of PV cell. R_s fundamentally depends on resistances of n and p bodies, contact resistance of metal base with p semiconductor layer, contact resistance of n layer with top metal grid, and resistance of grid. Resistance R_p is there majorly because of p–n junction's leakage current and is dependent on method of fabrication of PV cell. Normally value of R_p is high, however drop this parameter to make model lucid for analysis. R_s value is significantly low, and few times its value will also be not taken into the account. characteristics of I–V of PV cell depicted in Fig. 4 is dependent on external influences namely temperature and insolation range and on internal characteristics of device (R_s , R_p). Quantity of incident light directly show effect on the charge carriers generation and as a result, current generated by device. Determining current generated by light (I_{pv}) of elementary cells, without affect of parallel and series resistances is not easy.

The presumption $I_{sc} \approx I_{pv}$ is normally widely used in PV devices modelling because in pragmatic devices resistance in series is low and resistance in parallel is high. Current generated by light in PV cell is affected by temperature and linearly dependent on solar insolation by this equation.

$$I_{pv} = (I_{pv,n} + KI\Delta T) \frac{G}{G_n} \text{-----(4)}$$

where

$I_{pv,n}$ is current generated by light under nominal condition (usually 25 °C & 1000 W/m²)

$$\Delta T = T - T_n$$

T_n , T are nominal and actual temperatures [in Kelvin] respectively

G is insolation on device surface

G_n is nominal irradiation.

Dependence of diode saturation current I_0 on temperature can be determined by:

$$I_0 = I_{0,n} \left(\frac{T_n}{T} \right)^3 \exp \left[\frac{qE_g}{aK} \left(\frac{1}{T_n} - \frac{1}{T} \right) \right] \text{-----(5)}$$

here

I_0 is diode saturation current

E_g is semiconductor's bandgap energy ($E_g = 1.12$ eV for polycrystalline Si at 25°C)

$I_{0,n}$ is nominal saturation current:

$$I_{0,n} = \frac{I_{sc,n}}{\exp \left(\frac{V_{oc,n}}{aV_t,n} \right) - 1} \text{-----(6)}$$

Where $V_{t,n}$ is thermal voltage of N_s number of cells connected in series at nominal temperature, T_n . Saturation current I_0 of PV cells that comprise device is dependent on effective area of cells and on density of saturation current semiconductor (J_0). Current density, J_0 is dependent on intrinsic characteristics of PV cell, which depend on various physical parameters namely intrinsic carrier density, lifetime of minority carriers, coefficient of diffusion of electrons in semiconductor, etc. This sort of data is not generally ready for commercial PV arrays. Value of diode constant, 'a' can be chosen randomly. Various methods are there to calculate exact value of this constant. generally, $1 \leq a \leq 1.5$ and alternative is dependent on other parametric quantities of I–V model.

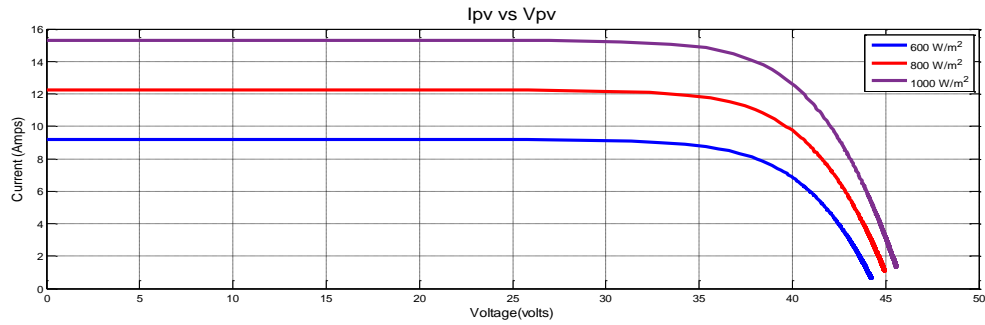


Fig 5: I vs V characteristics for varying irradiance

Fig 5 displays I-V characteristics of PV panel for change in Irradiance, we can see the Short circuit current getting reduced with decrease in irradiance. The three graphs shown are for three different irradiances like 600, 800, 1000 W/m^2 , and their corresponding I_{sc} are 9.5, 12.2, 15.5 respectively. We can also make a note that when current is becoming zero i.e., at open circuit condition for all three irradiances, the ambit of voltage is very small.

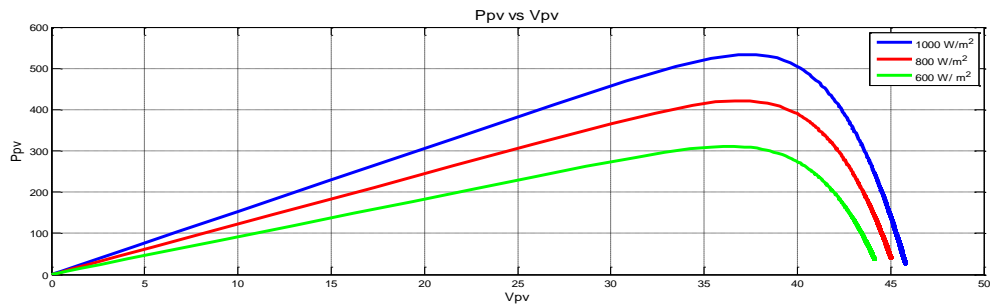


Fig 6: P vs V characteristics for varying irradiance.

Fig 6 displays P-V characteristics of PV panel for change in Insolation, we can see the Maximum power output of the panel getting reduced with decrease in irradiance. The three The three graphs shown here are for three different irradiances like 600, 800, 1000 W/m^2 , and their corresponding maximum powers are around 300, 425, 525 respectively, even in this figure we can notice at V_{oc} for all three irradiances the ambit of voltage is small.

2.3. Maximum power point tracking

Photo Voltaic cell has very poor efficiency. To enhance that parameter, there are methods to be followed to make load and source match in right way. One of those methods is Maximum Power Point Tracking (MPPT). The technique is used to extract maximum power that can be from a varying source. In photovoltaic systems, curve of I-V is nonlinear, resulting in difficulty to use it to power certain load. Some among the various algorithms are:

- Perturb and Observe scheme
- Incremental Conductance scheme
- Parasitic Capacitance scheme
- Constant Voltage scheme
- Constant Current scheme

2.3.1. Perturb and Observe scheme

The technique most commonly employed is Perturb and Observe (P&O). Advantage of this scheme is using very less number of sensors. Voltage at which panel is operating is sampled and this algorithm varies voltage at which panel is operating in desirable direction and samples $\frac{dP}{dV}$. If $\frac{dP}{dV}$ is positive value, then algorithm increases value of voltage in direction of MPP till $\frac{dP}{dV}$ is negative. Such iteration is performed continuously till algorithm attains MPP finally. Such algorithm is not desirable when variation in solar insolation is high. Voltage seldom attains an exact value, however perturbs in vicinity of maximum power point (MPP).

2.3.2. Incremental Conductance scheme

This scheme exercises incremental conductance $\frac{dI}{dV}$ of PV array to calculate sign of $\frac{dP}{dV}$. When $\frac{dI}{dV}$ is opposite and equal to value of $\frac{I}{V}$ (when $\frac{dP}{dV}=0$) algorithm senses that MPP is attained and hence it ends and reverts to corresponding value of operating voltage for operation to be in MPP. This scheme tracks varying insolation pattern more rapidly, and with more accuracy when compared to earlier scheme. The intricacy involved in this method is that it employs many sensors which is making it less beneficial economically.

$$P=V*I$$

Differentiating w.r.t voltage

$$\frac{dP}{dV}=d(V*I)/dV$$

$$\frac{dP}{dV}=I*\left(\frac{dV}{dV}\right)+V*\left(\frac{dI}{dV}\right)$$

$$\frac{dP}{dV}=I+V*\left(\frac{dI}{dV}\right)$$

When MPP is attained slope $\frac{dP}{dV}=0$. Hence condition would be

$$\frac{dP}{dV}=0$$

$$I + V * \left(\frac{dI}{dV}\right) = 0$$

$$\frac{dI}{dV} = -\frac{I}{V}$$

2.3.3. Parasitic Capacitance scheme

This scheme is an optimized variant of incremental conductance scheme, betterment obtained is by including the effect of PV cell's parasitic union capacitance into the voltage computation.

2.3.4. Constant Voltage scheme

This scheme is not widely in practice for the reason the losses during operation is dependent on relation between maximum power point voltage and open circuit voltage. Ratio of these two parameters is normally constant for a solar cell, it will be approximately 0.76. Hence open circuit voltage is obtained through experiment and voltage at which panel is operating is set to 76% of this value.

2.3.5 Constant Current scheme

Alike constant voltage scheme, this scheme depends on relation between maximum power point current and open circuit current. Ratio of these two parameters is normally constant for a solar cell, approximately about 0.95. Hence short circuit current is determined through experiment.

The aforementioned methods have obvious disadvantages and obvious advantages. Suitable method is to be Chosen regarding which algorithm to employ according to the necessity and operating conditions. For illustrating, if requirement is desired algorithm should be lucid and not much concerned about the reduction of ripple in voltage then P&O is apt. However, if the algorithm need to determine refined operating point and fluctuation of voltage near MPP should be decreased then IC method will be apt, which would result in intricacy in operation and less beneficial economically.

2.4. Flow charts of MPPT algorithms

Flow charts of mppt algorithms of two methods among the other described in previous subsection are shown in this section. Special emphasis is given to these two methods as they find much space in practice.

2.4.1. Flow chart for perturb and observe

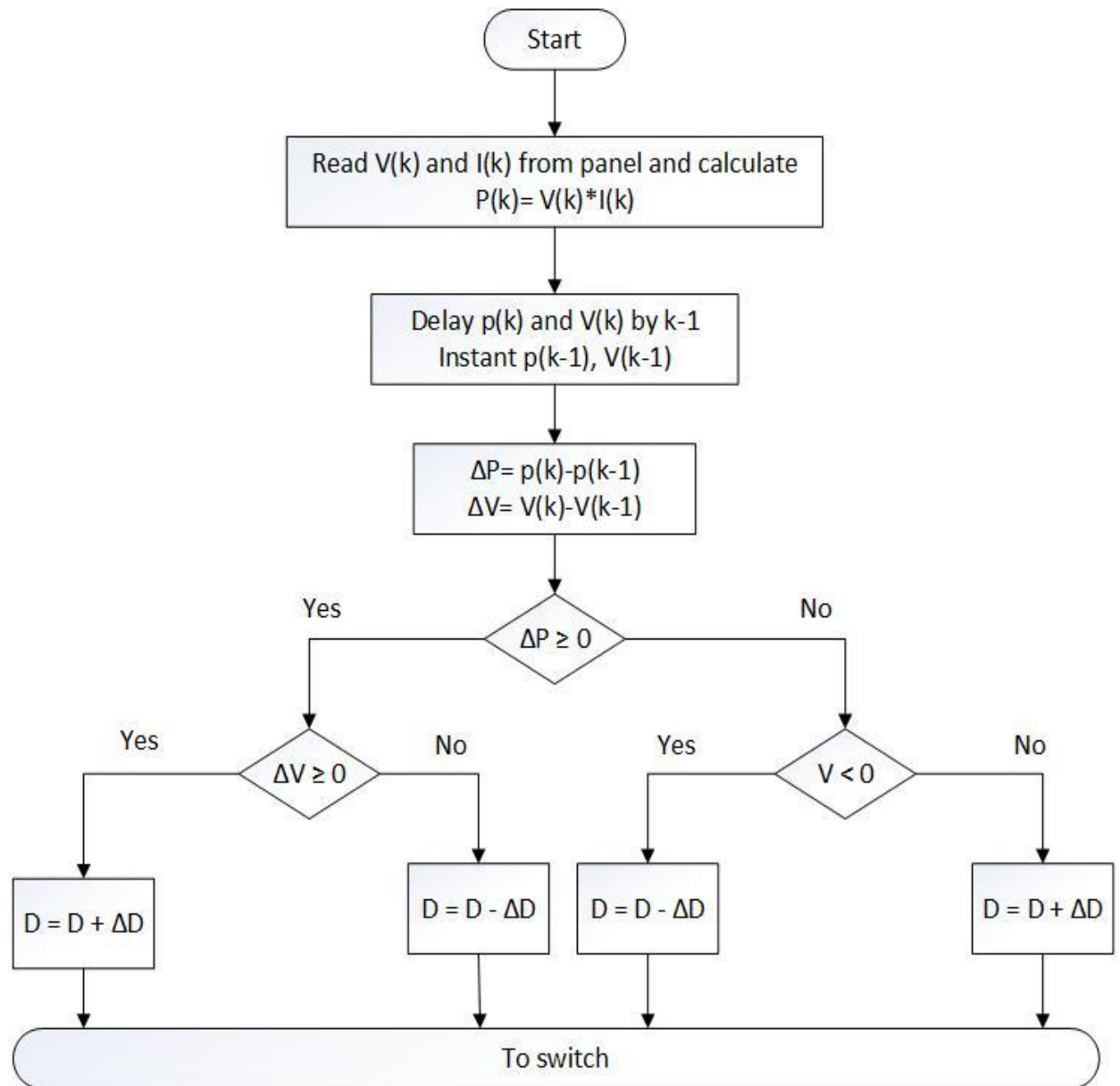


Fig. 7. Flow chart of P&O Algorithm

2.4.2. Flow chart of incremental conductance method

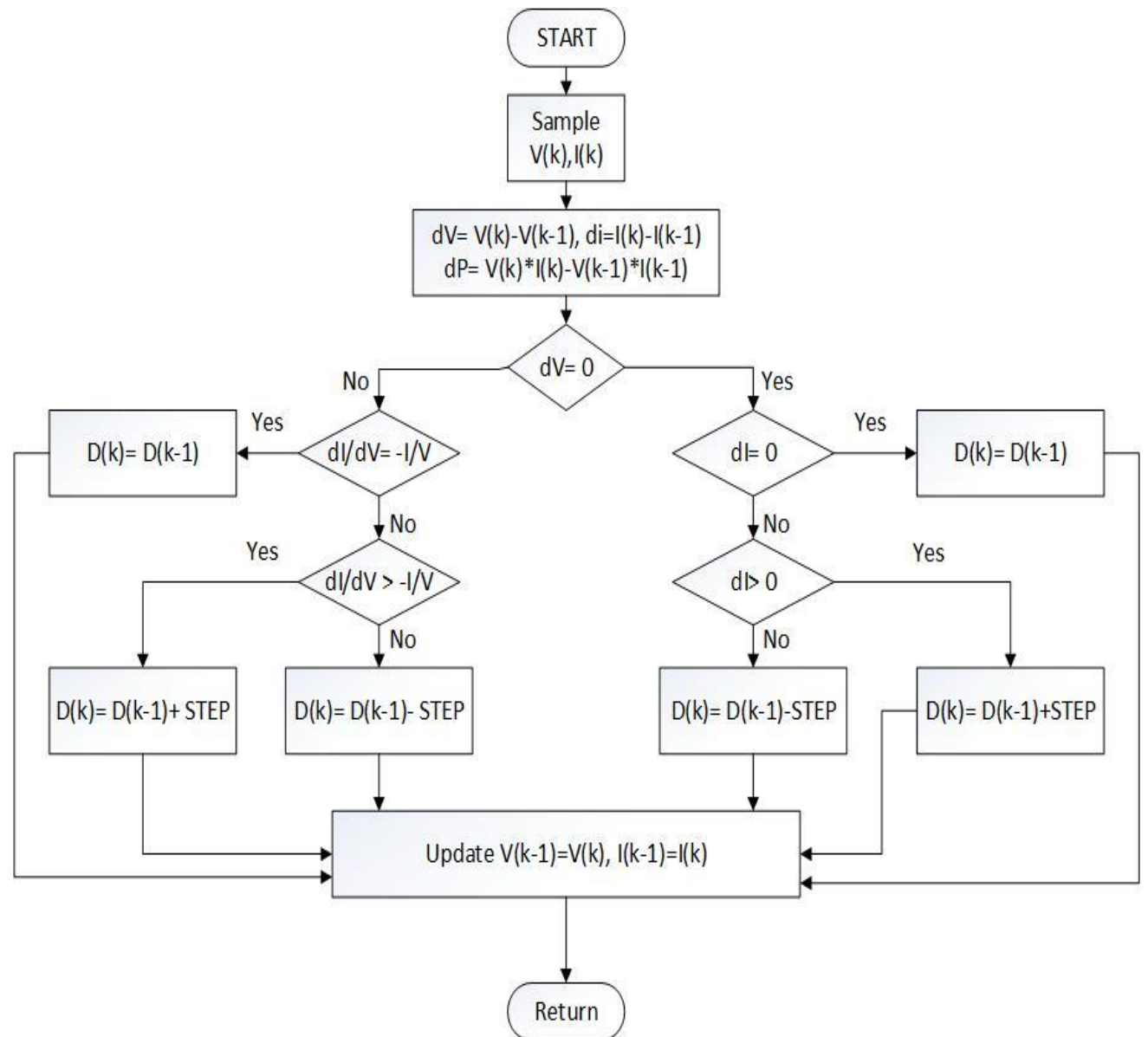


Fig. 8. Flow chart of Incremental Conductance Algorithm

Chapter 3

TCDIC (Transformer coupled dual input converter)

3.1. TCDIC operating principle

The topology of TCDIC is shown in Fig. 9. By having a look at figure. 9, one can infer that no specific converter is being used to ensure operation of PV array at MPP, which is resulting in the optimized usage of involved converters.

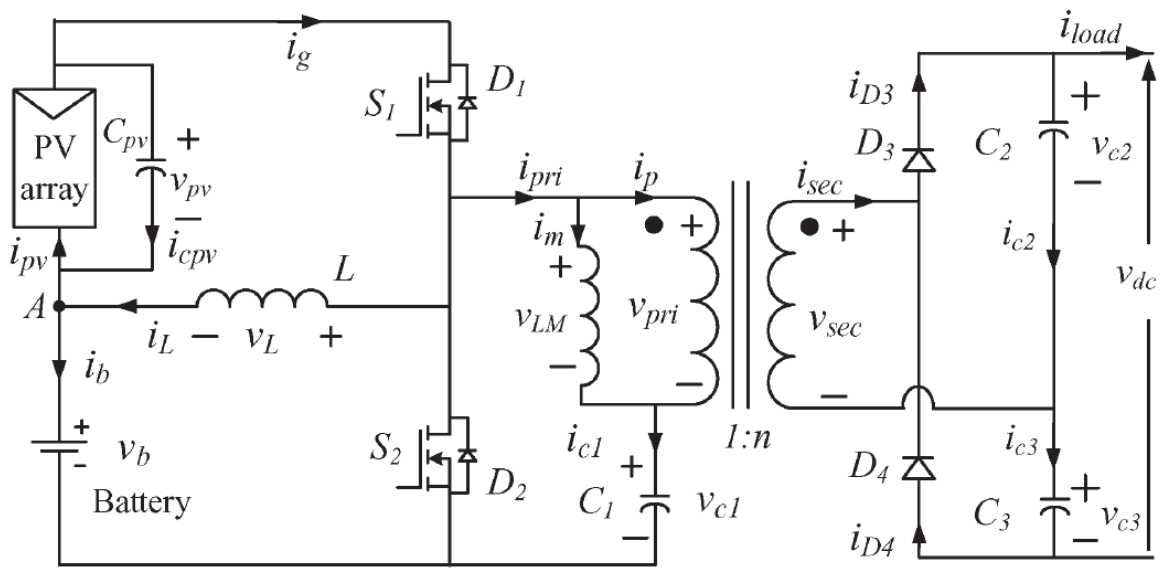


Fig. 9. Topology of the TCDIC

Moreover, in the path between battery and PV array only one converter stage is present, resulting in improvement of efficiency of battery charging process. Inductor current, i_L is designed to be continuous. S_1 and S_2 Switches will be operated in complementary fashion. In following analysis all passive elements and devices of semiconductor in the circuit are considered to be lossless in the

3.2. Modes of Operation

3.2.1. when inductor current, i_L is positive

Several modes of switching during this case are analysed in this sub section.

a) Mode I (conduction of D3 & S1): The instant at which S1 is switched on, voltage of pv panel, V_{pv} is subjected across L , leading to increase in inductor current \dot{i}_L . Throughout this time, voltage subjected across winding on the primary side of the transformer is $V_{pri} = (V_b + V_{pv} - V_{c1})$, where V_b is voltage of battery, V_{c1} is capacitor, $c1$ voltage. So, there will be an increase in current on primary of transformer, \dot{i}_{pri} and charging of capacitor, $c1$ takes place. There will also be an increase in Current flowing on secondary side winding of transformer, \dot{i}_{sec} . As diode, D3 is biased in forward direction, capacitor, $c2$ will charge. Voltage of $c2$ is determined as $V_{c2} = n (V_b + V_{pv} - V_{c1})$, where n is ratio of transformer turns. Tantamount diagram of circuit for this particular mode is figured in Fig. 10.

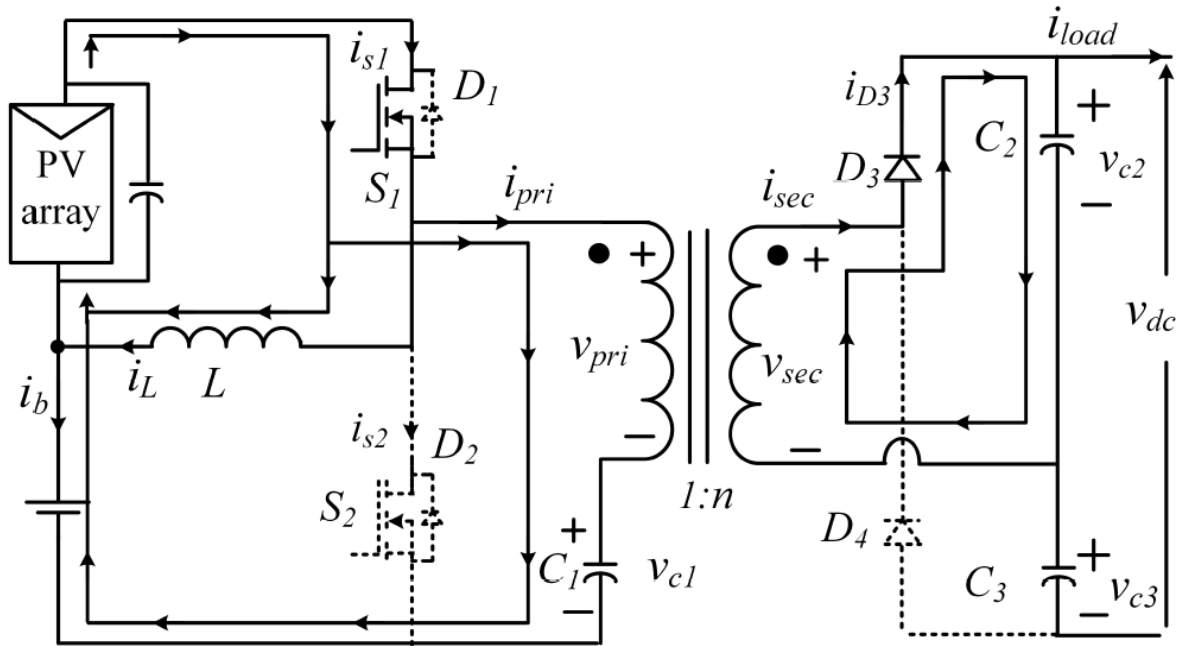


Fig. 10. Equivalent circuit diagram of TCDIC pertaining to mode I when inductor current is positive.

b) Mode II (conduction of D4 & D2): This mode of operation starts at the instant at which S1 is switched off and S2 is switched on. In beginning of this modeII, \dot{i}_L is positive, and as S1 is switched off, \dot{i}_{pri} is at zero. Because $\dot{i}_{pri} < \dot{i}_L$, diode D2 will start conducting. Voltage subjected on L is $V_L = -V_b$ and so, decrease in \dot{i}_L starts. Voltage subjected across primary winding of transformer is $V_{pri} = -V_{c1}$, and so, \dot{i}_{pri} goes to negative and decreasing of it starts, leading to $c1$ discharging. Current in transformer's secondary winding, \dot{i}_{sec} gets reversed, and turns on diode, D4. Charge across Capacitor, $c3$ is getting developed, and voltage of $c3$ will be given by $V_{c3} = (V_{c1}) * n$. while operation is in this mode, $(-\dot{i}_{pri}) < \dot{i}_L$ and diode, D2 is biased in forward direction. Operation under this mode

extends till \dot{i}_L equals $(-\dot{i}_{pri})$. Tantamount diagram of circuit for this particular mode is figured in Fig. 11.

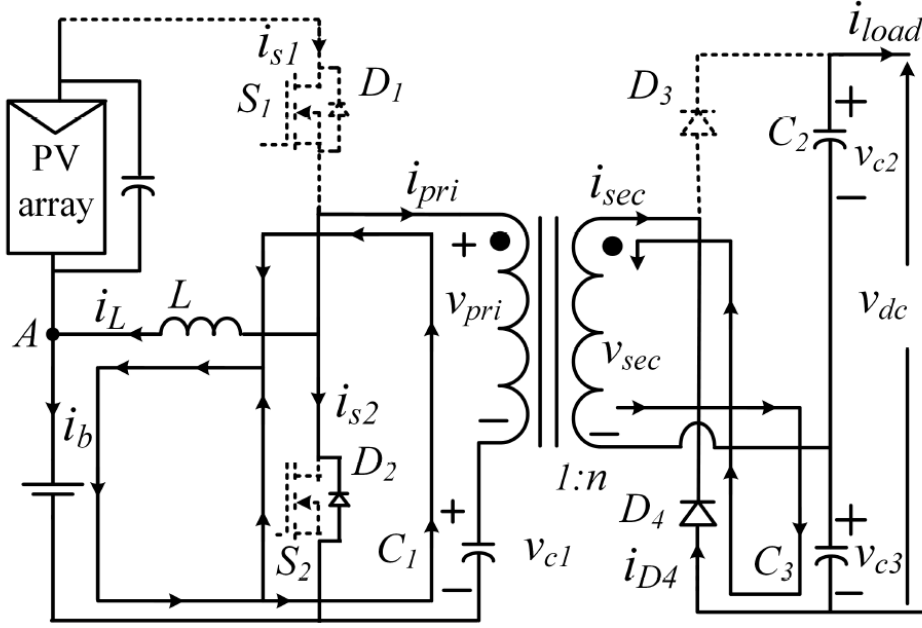


Fig. 11. Equivalent circuit diagram of TCDIC pertaining to mode II when inductor current is positive

c) Mode III (conduction of S2 & D4): The instant at which \dot{i}_L reaches less than $(-\dot{i}_{pri})$, diode, D2 is biased in reverse condition, and switch S2 conduction starts. Rest of the operation continues same as mode II. Tantamount diagram of circuit for this particular mode is figured in Fig. 12.

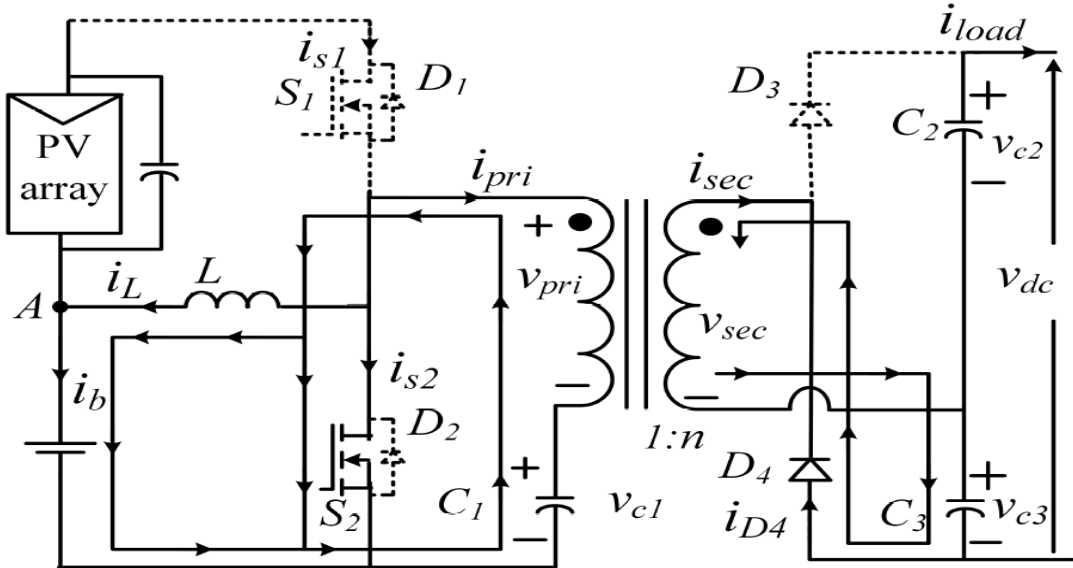


Fig. 12. Equivalent circuit diagram of TCDIC pertaining to mode III when inductor current is positive

3.2.2. when i_L is Negative.

d) Mode I (conduction of D_1 & D_3): This mode of operation starts at the instant S_1 is switched on and S_2 is switched off. In the beginning of this mode, i_{pri} is zero and i_L is in negative value. So, diode, D_1 conduction starts. The remaining operation is as same as mode I described in earlier sub section. This mode prolongs till i_{pri} is equal to $(-i_L)$. The tantamount diagram of circuit for this particular mode is figured in Fig. 13.

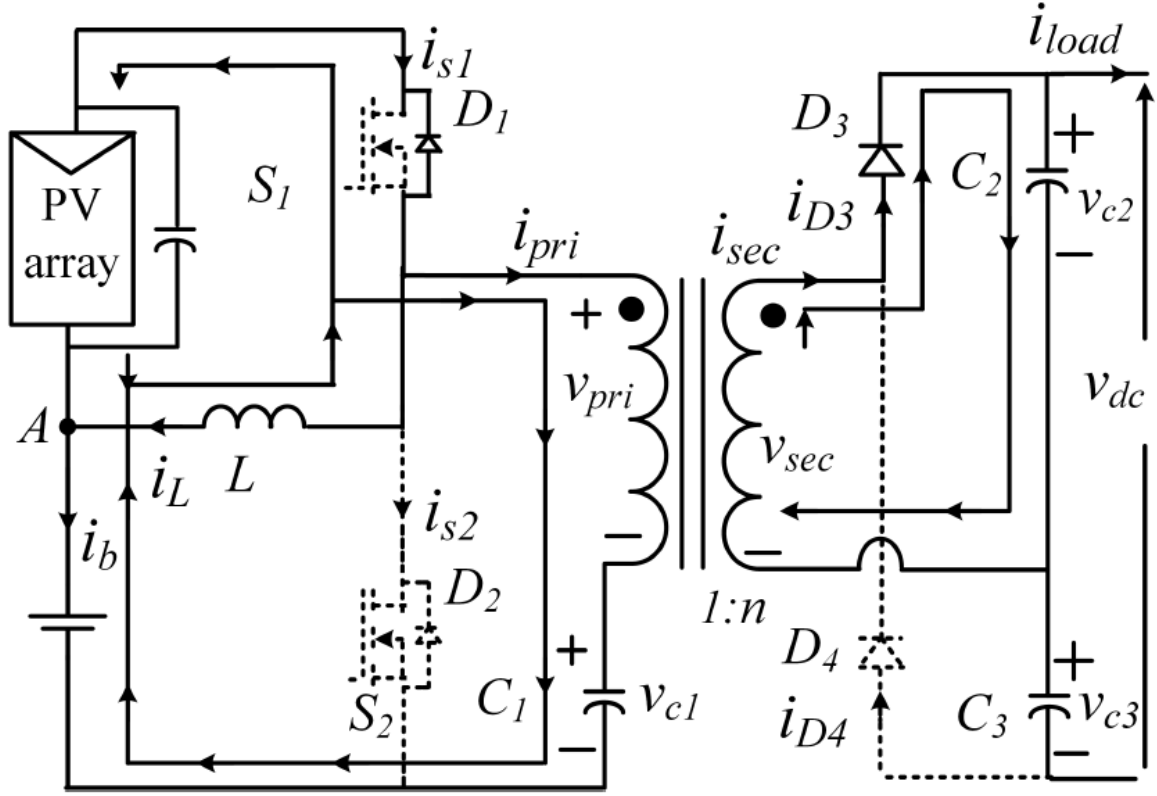


Fig. 13. Equivalent circuit diagram of TCDIC pertaining to mode I when inductor current is negative

e) Mode II (conduction of S_1 & D_3): When i_{pri} turns more than $-i_L$, diode D_1 is biased in reverse condition, and conduction of switch, S_1 starts. The remaining part of operation is as same as mode I described in earlier sub section. Tantamount diagram of circuit for this particular mode is figured in Fig. 14.

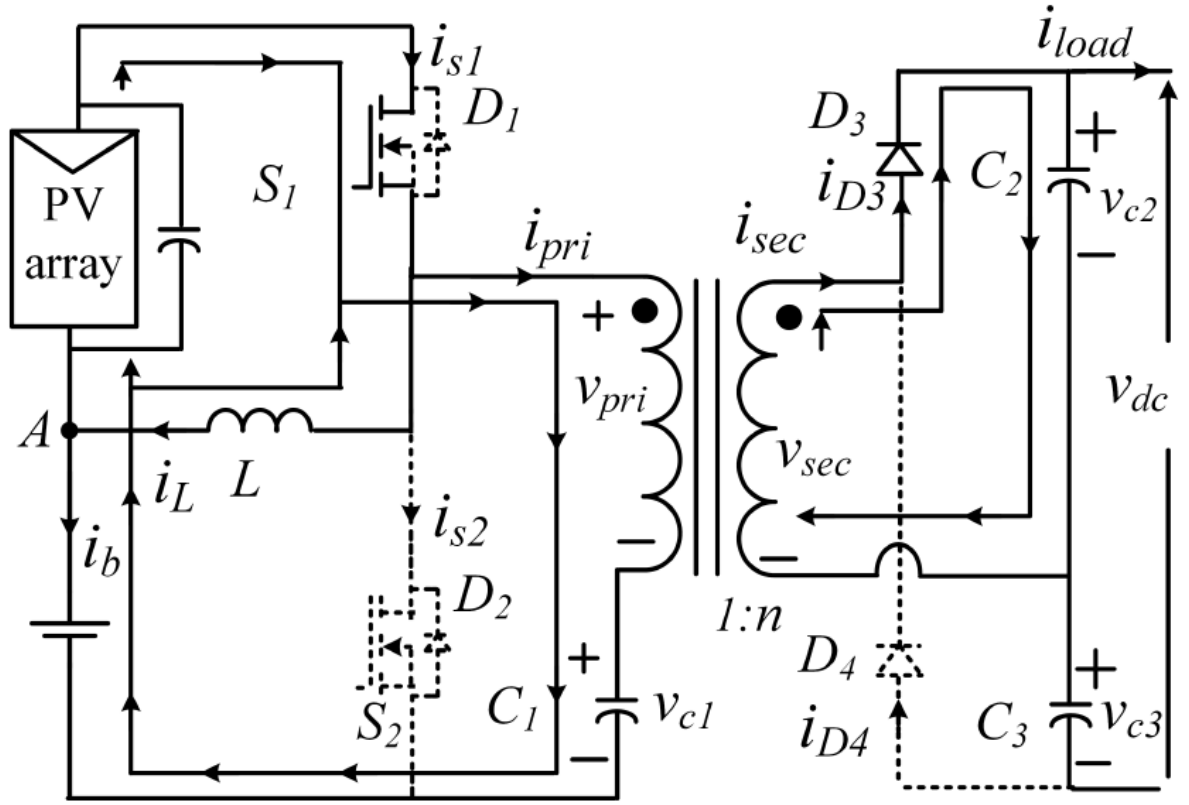


Fig. 14. Equivalent circuit diagram of TCDIC pertaining to mode II when inductor current is negative

f) Mode III (S2 & D4 conducting): This mode of operation starts at the instant S1 is switched off and S2 is switched on. In this mode, both i_{pri} and i_L are negative in direction, and conduction of switch, S2 begins. Current in negative direction of transformer's primary winding leads to negative current in transformer's secondary winding. So, diode D4 is biased in forward direction and capacitor C3 gets charged. In this mode, $V_{pri} = -V_{c1}$, $V_{c3} = nV_{c1}$ and $V_L = -V_b$. Tantamount diagram of circuit for this specific mode is as same as which is figured in Fig. 11, excluding the i_L direction which is reversed.

From Fig. 9, voltage across the inductor L, V_L is given as

$$V_L = V_{pv}, \text{ for } S1 \text{ on}$$

$$V_L = -V_b, \text{ for } S2 \text{ on.} \text{-----(7)}$$

So, average voltage across inductor is

$$V_L = DV_{pv} - (1 - D)V_b$$

Here D is switch S1 duty cycle. Equating average voltage across inductor to zero,

$$V_{pv} = \left[\frac{(1-D)}{D} \right] V_b \text{-----(8)}$$

From (8), we can note that panel voltage V_{pv} can be regulated by adjusting D , as voltage of battery, V_b can be considered to be stiff source. So, PV array operation at MPP can be obtained by thorough adjustment of D .

TCDIC average output voltage, V_{dc} can be determined by

$$\begin{aligned} V_{dc} &= (V_{c3} + V_{c2}) \\ &= [nV_{c1} + n(V_{pv} + V_b - V_{c1})] \\ &= n(V_{pv} + V_b) \end{aligned} \quad (9)$$

By applying KCL at point A in Fig. 1

$$i_{cpv} + i_L = i_{pv} + i_b \quad (10)$$

Assuming average values of i_{pv} , i_{cpv} , i_L and i_b over one switching cycle and noticing that $\bar{i}_{cpv} = 0$, leads to transformation of (10)

$$i_b = i_L - i_{pv} \quad (11)$$

From (11), Our inference will be, when $i_{pv} < i_L$, battery will be charged, and when $i_{pv} > i_L$, discharging of battery takes place. So, by regulating i_L , for a fixed i_{pv} , charging of battery and discharging of battery can be regulated. Drawback of this topology (TCDIC) and the linked up constraints of design are elaborated in [13]. Section 3.4 deals in elaboration of Control scheme for TCDIC.

3.3. Mathematical model of TCDIC based on small signal analysis

For designing closed loop controllers, a mathematical model of the TCDIC based on small signal analysis is deduced [13]. These annotations are taken to develop the model: Average value of variable x over one switching cycle where X is its steady-state value is \bar{x} , and small signal perturbation of x around its steady-state value X is represented by \hat{x} .

Equations depicting behaviour of system in steady state condition are

$$\bar{V}_L = d\bar{V}_{pv} - (1 - d)\bar{V}_b$$

$$\bar{i}_{cpv} = \bar{i}_{pv} - \bar{i}_g = \bar{i}_{pv} - d(\bar{i}_L + \bar{i}_{pri})$$

$$\bar{V}_{LM} = (\bar{V}_b + \bar{V}_{pv} - \bar{V}_{c1})d - \bar{V}_{c1}(1 - d)$$

$$\bar{i}_{c1} = \bar{i}_{pri} = \bar{i}_m + \bar{i}_p$$

$$\bar{i}c2 = \frac{\bar{i}pv}{n}d - \bar{i}load$$

$$\bar{i}c3 = -\bar{i}load = (1 - d)\left(\frac{\bar{i}p}{n}\right)$$

$$\bar{i}c2 + \bar{i}c3 = \frac{\bar{i}p}{n} - 2\bar{i}load = C2 \frac{d\bar{V}c2}{dt} + C3 \frac{d\bar{V}c3}{dt}$$

Assuming $C2=C3=C$

$$C \frac{d(\bar{V}c2 + \bar{V}c3)}{dt} = \frac{\bar{i}p}{n} - 2\bar{i}load$$

$$C \frac{d\bar{v}dc}{dt} = \frac{\bar{i}p}{n} - 2\bar{i}load$$

To make system linear, a small perturbation is enforced around a steady state point such that all variables i_{pri} , i_{pv} , d , i_L , v_{pv} , i_{load} , i_m , i_p , v_{dc} , i_{c1} , i_{c2} and i_{c3} get perturbed in coming form:

$$x = \hat{x} + X$$

where in $X \gg \hat{x}$, following are the equations of linearized system

$$Ls\hat{i}_L = D\hat{V}_{pv} + (V_{pv} + V_b)\hat{d} \text{-----}(12)$$

$$\hat{V}_{pv} \left[sC_{pv} + \frac{1}{R_{pv}} \right] = -\hat{d}(I_L + I_{pri}) - D(\hat{i}_L + \hat{i}_{pri}) \text{-----}(13)$$

$$sL_m \frac{d\hat{i}_m}{dt} = (V_b + V_{pv})\hat{d} + \hat{V}_{pv}D - \hat{V}_{c1} \text{-----}(14)$$

$$\hat{i}_{c1} = \hat{i}_m + \hat{i}_p \text{-----}(15)$$

$$sC2\hat{V}_{c2} = \hat{i}_{c2} = \frac{1}{n}[D\hat{i}_p + I_p\hat{d}] - \hat{i}_{load} \text{-----}(16)$$

$$sC3\hat{V}_{c3} = \hat{i}_{c3} = \frac{1}{n}[(1 - D)\hat{i}_p - \hat{d}I_p] \text{-----}(17)$$

$$\hat{V}_{dc}[Cs + \frac{2}{R}] = \frac{1}{n}\hat{i}_p \text{-----}(18)$$

where $R = V_{dc}/I_{load}$ and $R_{pv} = -(V_{pv}/I_{pv})$. The transfer functions which are necessary are found by resolving (12) – (18).

$$\frac{\hat{V}_{pv}}{\hat{d}} (\hat{v}_0 = 0) = - \frac{LCLmLs^3 + CD(V_{pv} + V_b)(Lm + L)s^2 + LILs + D(V_{pv} + V_b)}{C_{pv}CLms^4 + \frac{LCLm}{R_{pv}}s^3 + [C_{pv}LR_{pv} + D^2CLm + CD^2] + \frac{L}{R_{pv}}s + D^2} \text{-----}(19)$$

$$\frac{\hat{i}_L}{\hat{d}} (\hat{v}_0 = 0) = \frac{(CLms^2 + 1)[(V_b + V_{pv} - ILDR_{pv}) + (V_{pv} + V_b)sR_{pv}C_{pv}]}{R_{pv}CC_{pv}LLms^4 + LCLms^3 + R_{pv}[LC_{pv} + D^2C(Lm + L)]s^2 + Ls + D^2R_{pv}} \text{-----}(20)$$

3.4. Control Strategy

The controller employed in standalone schemes is needed to deliver the following duties

- 1) Maximum power extraction from PV array.
- 2) Adjusting battery use without breaching overcharge limit and over discharge limit.
- 3) Dc to ac conversion while keeping the voltage at load at desired level.

A controller is described for adjusting TCDIC to realize first two above mentioned duties, but the third requirement is obtained by incorporating a normal proportional integral (PI) controller to control voltage on output side of full bridge inverter through sinusoidal pulse width modulation. As normal control scheme is employed to control voltage on output side of inverter, design parameters of it are not given here. Particulars of algorithm to control TCDIC are discussed here. To obtain these coveted practicalities, TCDIC should be operated in any one of following modes at a specific instant of time.

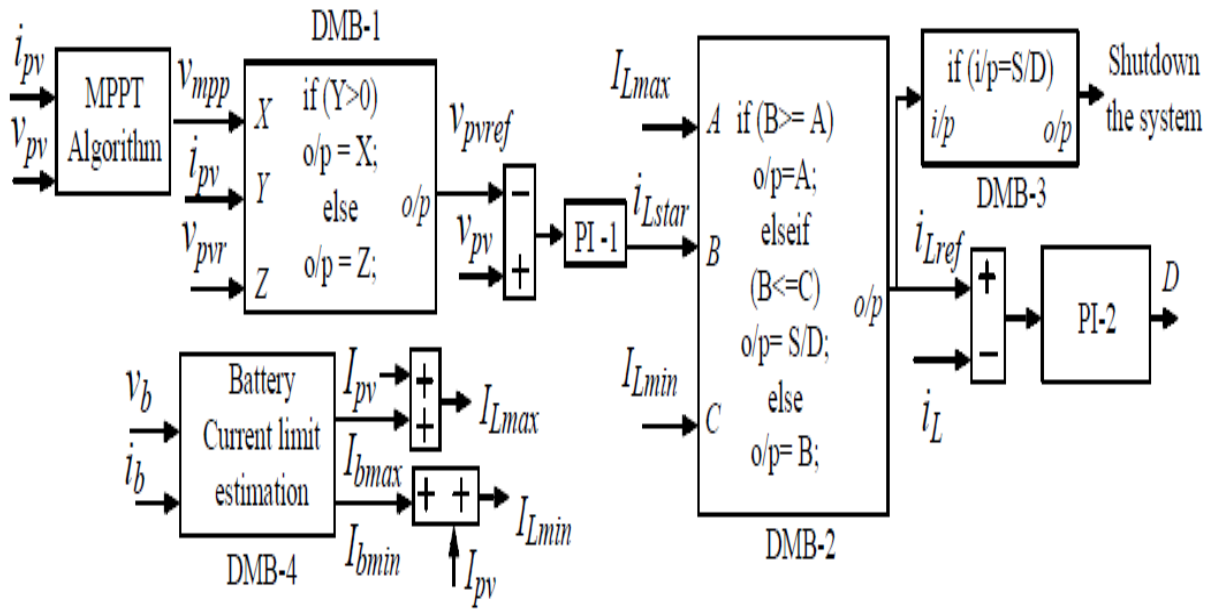


Fig. 15. Control strategy for the TCDIC

- 1) MPPT mode of operation: When system is operating under this mode, maximum power is extracted from PV array. However, for operation to be in this mppt mode, any one of the following preconditions should be met:
 - 1) The available maximum PV power, P_{mpp} is greater than load demand, P_l and extra power can be used to charge battery without getting overcharged.
 - 2) $P_l > P_{mpp}$ and battery having the capacity to feed $(P_l - P_{mpp})$ amount of power without getting over discharged.

In MPPT mode PV power is determined by $P_{pv} = P_{mpp} = (P_l + P_b)$, here P_b is the power of battery that is taken positive while charging and negative during discharging.

- 2) Non MPPT mode of operation: Dependent on battery's state of charge (SOC) value, its current sent in to charge should be curtailed to a maximum allowable limit I_{bmax} to avoid battery getting damaged because of overcharging phenomenon. This I_{bmax} limits the amount of power that can be sent into the battery to value of $P_{bmax} = V_b * I_{bmax}$. In the case of $P_l < P_{mpp}$ and the extra power is greater than P_{bmax} , we cannot make the system operate under mppt mode which will lead to overcharging of battery. Under this case, power taken from PV array is decreased just to a value $P_{pv} = (P_l + P_{bmax})$. Hence this mode is called non mppt mode of operation.
- 3) Battery only (BO) mode of operation: System comes into this mode of operation when power from PV array is zero and existing load demand at that instant can be supplied through battery only with keeping a note on over discharging limit.
- 4) Shutdown mode: In the case of $P_l > P_{mpp}$ and battery not having the necessary capacity to deliver $(P_l - P_{mpp})$ amount of power, it is imperative to shut down the system to avoid the over discharging phenomenon of battery.

This control scheme which is used for selecting suitable operation mode of TCDIC, is dependent on amount of battery's SOC, the accessibility of power from PV array, is figured in Fig. 15. Suitable selection of mode will be performed by four logical decision making blocks (DMBs). DMB-1 control block sets reference of voltage of PV array (V_{pvref}). It also determines whether the system should operate in MPPT mode or BO mode. Maximum power point tracking mode of operation is selected when it is noted that $i_{pv} > 0$, here by representing the PV power availability and Maximum Power Point Tracking algorithm block output (i.e., V_{mpp}) sets V_{pvref} . under the case of absence of PV power, battery only mode is chosen and V_{pvref} is considered as V_{pvr} , where this parameter is selected to keep Dc link voltage V_{dc} in the prescribed ambit of 350 to 460 volts according to (9). i_{Lstar} , needed reference for inductor current is set by passing the error between V_{pv} and V_{pvref} to PI controller. The lower limit, I_{Lmin} and upper limit, I_{Lmax} is enforced on i_{Lstar} to avoid over discharging or over charging phenomena of batteries. (11)

These two limits can be given by

$$I_{Lmax} = I_{pv} + I_{bmax} \text{-----}(21)$$

$$I_{Lmin} = I_{pv} + I_{bmin} \text{-----}(22)$$

Here I_{bmin} and I_{bmax} are the maximum permissible discharging and charging currents of battery respectively. Particularly these limits will be decided based on Discharge depth and

SOC status of battery [14]. DMB-4 block is used to perform the above mentioned duties. DMB-2 block decides level of reference of inductor current i_{Lref} after resolving the constraints brought by I_{Lmin} and I_{Lmax} . Operation of system either in BO mode when $i_{pv} \leq 0$ or MPPT mode when $i_{pv} > 0$ when i_{Lref} stays in its ordained bound. System shuts down when the DMB-3 block takes back gate pulses from all switches when i_{Lref} reaches its beneath bound signalling the battery over discharge bound is arrived. i_{Lref} reaches its zenith when overcharging bound of the battery is reached, whereas this case is possible only when system is under MPPT mode of operation ($P_l < P_{mpp}$) and that extra power is higher when compared with P_{bmax} . At this condition, i_{Lref} is restricted to I_{Lmax} to restrict flowing into battery (current which is charging) to I_{bmax} , and MPPT is bypassed. As charging current of battery is restricted to I_{bmax} , absorbed power by the battery is limited to P_{bmax} . This results in power available from PV greater than $(P_{bmax} + P_l)$.

This surplus power from PV will start charging capacitor of PV panel, hence there will be an increase in its voltage more than V_{mpp} , which shifts PV array operating point towards right of MPP, and there will be a decrease in power obtained from the PV panel. This action extends till PV array power again reaches $(P_{bmax} + P_l)$. The PV array will be operating on the right of its true MPP ($P_{mpp} > P_{pv}$), while system is operating under non MPPT mode. When there will be reduction in demand of load when under non MPPT mode of operation, power obtained from PV array reaches greater than $(P_{bmax} + P_l)$, and this extra power obtained will start charging capacitor of PV, resulting in shifting of PV panel operating point more towards right side of its earlier point of operation. If the case of increase in load demand considered, power obtained from PV array will not be able to deliver increased load demand. So, PV capacitor and dc link capacitors discharging will be started. When the PV capacitor voltage reduces, the point of operation of PV array moves towards left from its earlier point of operation. This results in an increase in the power obtained from PV array, and this phenomenon will continue till is restore in balance of power. If load demand is increased to a limit so that available power from PV panel at its MPP cannot be supplying increased load demand, battery will come out of charging mode, i_{Lref} will reach a value which is less when compared to I_{Lmax} , and the system reaches Maximum Power Point tracking mode of operation.

Chapter 4

Battery charge security

This chapter discusses the scheme to assure high state of charge of a battery and to ensure avoiding overcharging phenomenon of battery by envisioning a consecrated algorithm which is expected to meet following objectives.

- 1) how expeditiously it can obtain energy which is stored in batteries when power from PV panel is not meeting the demand.
- 2) how expeditiously it can pump energy into the batteries when there is surplus power from PV panel.

4.1. Lead Acid Battery modelling

Accessibility of a conventional charge voltage model, that is fitted to data from experiment, is crucial to comprehend operation of batteries under varying realistic conditions. These days, a fractional order modelling was developed for estimating resistance of the battery. Other way comprises of employing an extended Kalman filter to observe parametric quantities of battery. A charge voltage model can also be employed for conception of charge control, regulation system, , and global advanced PV control system with consecrated control functions for grid. In this scenario, most widely used models are electro circuit models, that are electrical circuit elements based, namely voltage source, resistors and capacitors. Different electro circuit models for simulation of behaviour of battery are available, and these models have varying amounts of intricacies and simulation characters.

But, among the available models, not many or none is conceived to be acceptable in terms of intricacy precision. Intricacy is because of the parameters to be found are high in number. The crucial results show that, for every battery, the parametric quantities are dissimilar and this is the main trouble for the general PV simulation or regulation system design. Hence, it is preferred to have a generic model with constant parameters that is effectual for any battery size. In this scenario, in [15], a normalized model is discussed. This model is lucid, for the reason the experimental identification of empirical parameters is not needed. Results that were obtained for different batteries in [15] and [17], figure out that model can decently reproduce behaviour of batteries under charging/discharging is taking place.

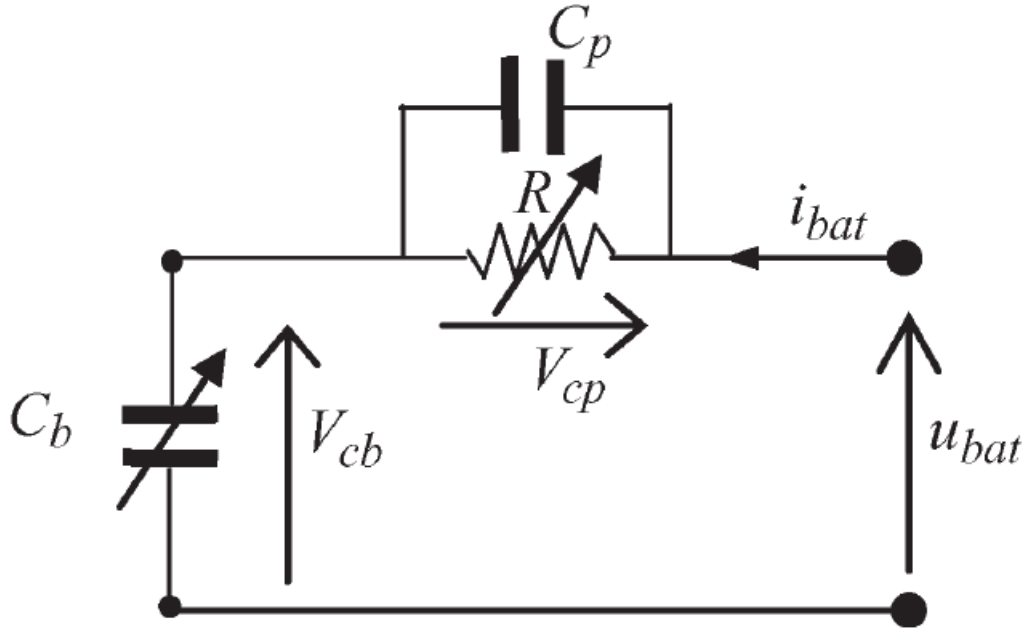


Fig. 16. Battery equivalent circuit.

To avoid excessive complexity, A Lucid capacitor- resistor electrical model is taken into the consideration as shown in Fig. 16, and its voltage at terminals can be determined by

If $U_{bat} < nV_g$

$$U_{bat}(t) = n(V_{cb}(t) + V_{cp}(t)) \text{-----(23)}$$

$$\frac{dV_{cb}}{dt} = \frac{i_{bat}(t)}{C_b(t)} \text{-----(24)}$$

$$\frac{dV_{cp}}{dt} = -\frac{1}{R(t)C_p} V_{cp} + \frac{i_{bat}(t)}{C_p} \text{-----(25)}$$

$$SOC(t) = \frac{V_{cb}(t)-2}{0.16} \text{-----(26)}$$

If $U_{bat} \geq nV_g$

$$U_{bat}(t) = n (V_{cb}(t) + R(t) i_{bat}(t)) \text{-----(27)}$$

$$SOC(t) = 1 \text{-----(28)}$$

$$V_{cb}(t)=2.16v \text{-----(29)}$$

With

$$R(t) = \frac{1}{C_{10}} \left(\frac{6}{1+i_{bat}^{0.6}(t)} + \frac{0.48}{\left(1 - \frac{(V_{cb}(t)-2)}{0.16}\right)^{1.2}} \right) \text{-----(30)}$$

$$C_b(t) = \frac{1.67C_{10}}{1 + 0.67\left(\frac{i_{bat}(t)}{I_{10}}\right)^{0.9}} \frac{1}{n^{0.16}} \text{-----}(31)$$

$$I_{10} = \frac{C_{10}}{10} \text{-----}(32)$$

Here, i_{bat} is current through battery, u_{bat} is voltage of battery, n is number of cells, R is internal resistor, V_{cb} is electromotive force, V_{cp} is polarization voltage, $V_g = 2.35$ V is gassing voltage, C_{10} is nominal capacity after a duration of 10 hours charging, I_{10} is charge current corresponding to C_{10} and C_p is polarization capacitor

4.2. Current Tracking of battery

The algorithm for current tracking of battery is to ascertain reference current for battery. Three major points what we have to note are

1) When battery is charging, if current of battery is kept high constantly, then voltage of battery increases in fast manner till it attains a gassing voltage ($V_g = 2.35$ V). When voltage of battery crosses this parameter, exuberant pressure of gas may develop in the battery. This gas can escape through safety valves, that in turn reduces lifetime of battery, and there are chances for an explosion to take place.

2) While charging of the battery is taking place, internal resistor still is dependent on SOC of battery. when SOC of battery is high, there will be high rate of increase in value of that internal resistor. So under scenario, even with a constant current of battery, the losses in battery are more crucial. Repercussion is efficiency of battery is low.

3) When empty battery is considered, with constant current of battery, (say $i_{bmax} = C_{10}/5$), SOC of battery will reach only about 70%. With constant current through battery (say $i_{bmin} = C_{10}/100$), SOC of battery will reach around 95%, however time of charging increases compared to earlier case.

To assure a high SOC of battery, less charging time, high efficiency and security against overcharging it is imperative to decrease losses of battery and to maintain voltage of battery less than gassing voltage. This can be evinced through below considerations:

$$I_{bat_ref}(t_o + \Delta t)R(t_o + \Delta t) \leq I_{bat_ref}(t_o)R(t_o) \text{-----}(33)$$

$$U_{bat}(t_o) < nV_g \text{-----}(34)$$

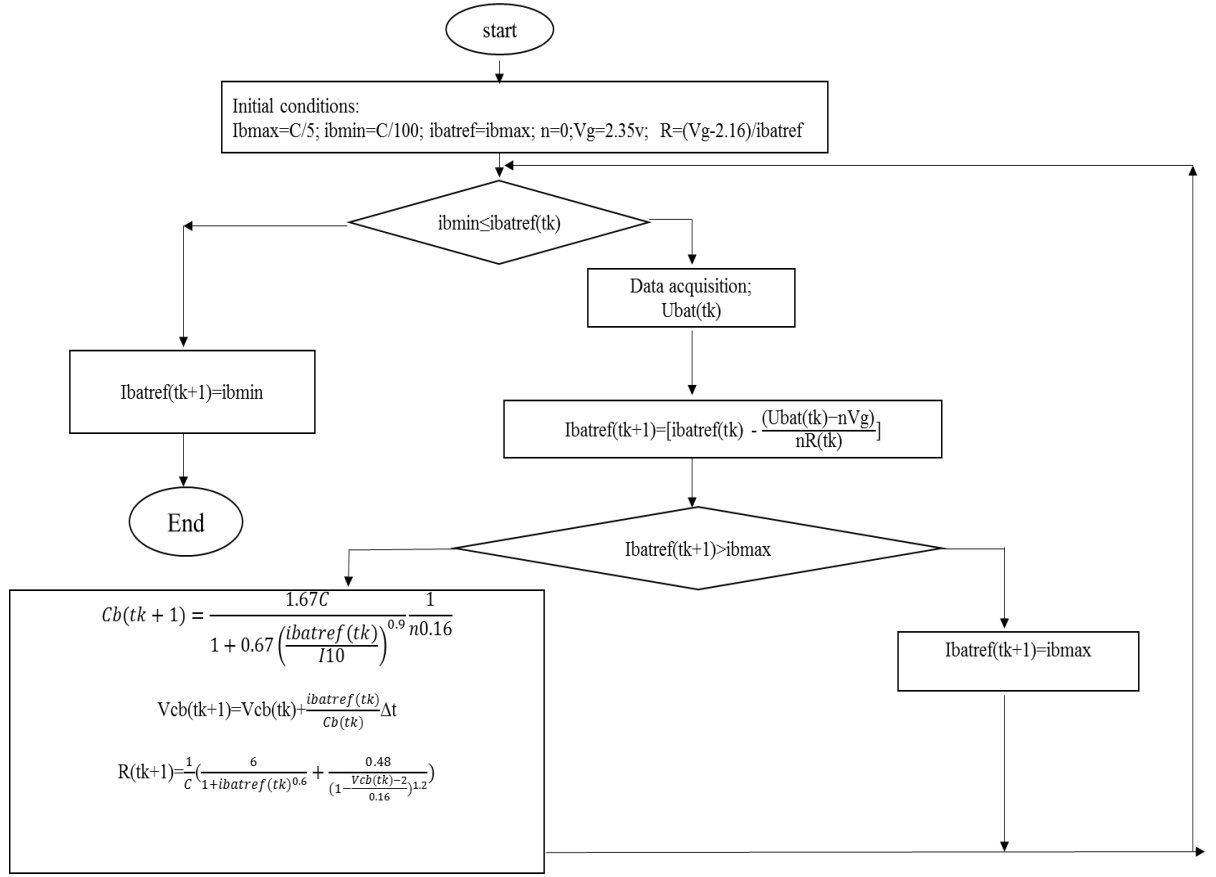


Fig. 17. Battery current tracking algorithm flowchart

Adding all these equations gives one relation i.e.,

$$I_{bat_ref}(to+\Delta t) < \left[\frac{nV_g - U_{bat}(to) + I_{bat_ref}(to)R(to)}{R(to+\Delta t)} \right] \text{-----}(35)$$

Because the variations in internal battery resistor are slow [in (28)], this relation can be made lucid like:

$$I_{bat_ref}(to+\Delta t) < \left[\frac{nV_g - U_{bat}(to)}{R(to)} + I_{bat_ref}(to) \right] \text{-----}(36)$$

From (27), when voltage of battery u_{bat} attains gassing voltage V_g , internal resistor of battery can be approximated from (37):

$$R(to) = \frac{V_g - 2.16}{I_{bat_ref}(to)} \text{-----}(37)$$

So, the method employed comprises of battery loading with a maximum current in beginning and then reducing it corresponding to discussed current tracking algorithm of battery.

Chapter 5

Simulation Results and Discussions

Complete diagram of standalone system which is displayed in Fig.18 is simulated in Matlab_Simulink. Results of simulation under different operating conditions are shown and discussed in present chapter. Different parametric quantities with which simulation is done are mentioned in Table I.

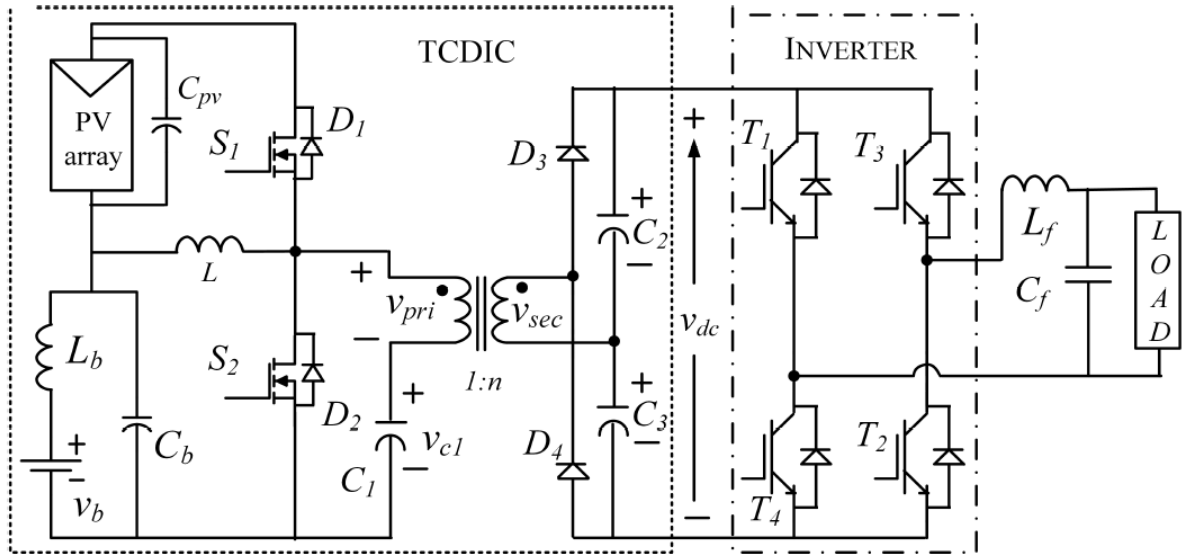


Fig. 18. Complete stand-alone scheme.

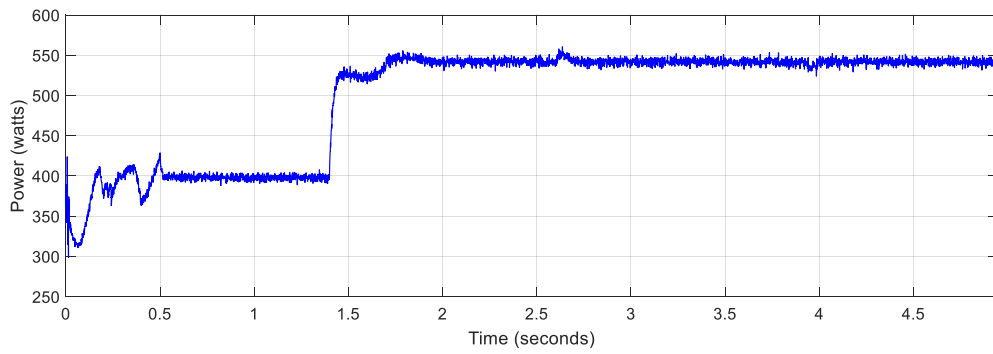
Table I: Parameters with which Simulation performed

Parameter	Its value
Switching Frequency	15KHz
MPPT Algorithm	Perturb & Observation
Inductors	Lb=1 mH, L= 3mH, Lf= 2.5mH
Capacitors	Cpv=2000μF, Cb=1000 μF, Cf=8 μF, C1=8 μF, C2=C3=1000 μF
PI Controller gains	For PI-I; Kp=0.068, Ki=2.5 For PI-II; Kp=0.03, Ki=1
Transformer turns ratio	n=6
Power rating	500 VA

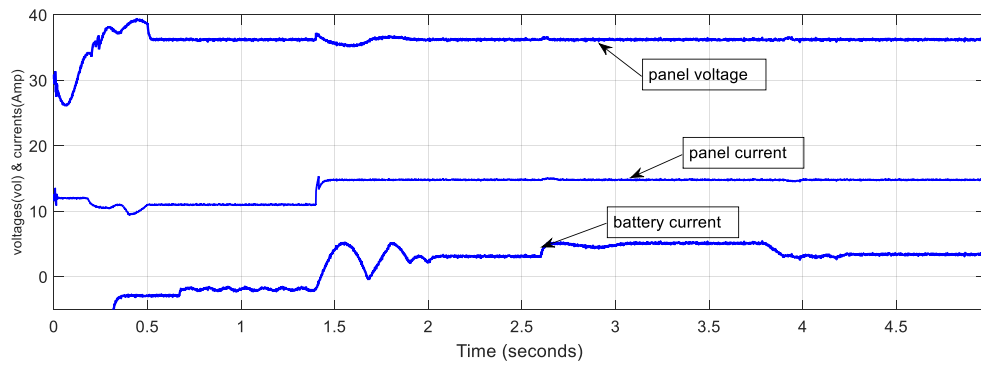
5.1.Under changes in load and irradiance level during MPPT mode.

Table II: Parameters with which simulation is performed for changes in load and irradiance level during MPPT mode.

Time(in seconds)	Irradiance Levels(KW/m^2)	Load Demand(watts)
0-1.4	0.75	450
1.4-2.6	1	450
2.6-3.8	1	350
From 3.8	1	450



(a)



(b)

Fig. 19. Waveforms of P_{pv} , V_{pv} , i_{pv} , and i_b of the system for changes in load and irradiance level during MPPT mode.

Waveforms of system simulated under variations in irradiance level and load when it is in MPPT mode of operation are displayed in Fig. 19 and Fig 20. In the beginning, the irradiance level was given a value of $0.75 \text{ kW}/\text{m}^2$ ($V_{mpp} = 35.4 \text{ V}$, $I_{mpp} = 11 \text{ A}$). At 1.4 seconds, irradiance level is varied to $1 \text{ kW}/\text{m}^2$ ($V_{mpp} = 36 \text{ V}$, $I_{mpp} = 14.8 \text{ A}$).

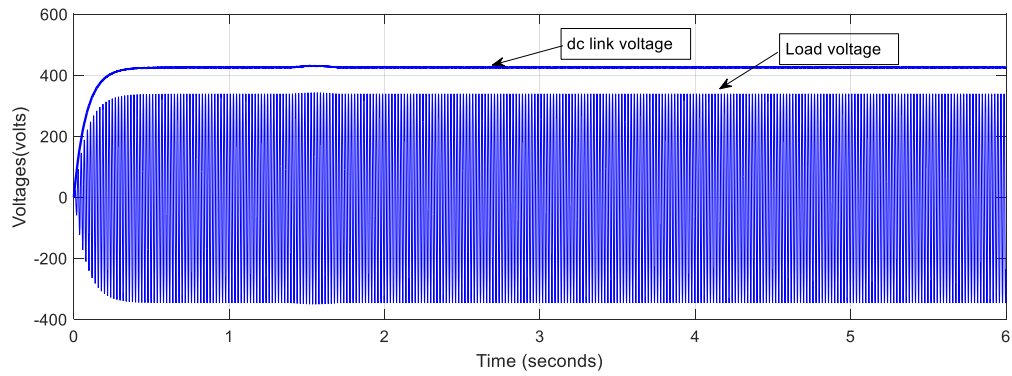


Fig. 20. Waveforms of V_{dc} and load voltage of the system for changes in load and irradiance level during MPPT mode.

The load demand is varied as follows: From 0 to 2.6 seconds it is 450 W, from 2.6 to 3.8 seconds it is 350 W, 450 W from 3.8 seconds. From Fig.19 (a) We can note that till 1.4 seconds when the insolation is at 0.75 kW/m², the load demand is greater than pv power, so battery is discharging to meet that extra load demand, once the insolation at 1.4 seconds is increased, PV power is greater than load demand, so this extra power goes into battery to charge it. At 2.6 seconds when load demand is further decreased, the power going into the battery got increased, again at 3.8 seconds when load demand is increased to 450W, the power going into the battery gets decreased. From Fig. 19 (b) that V_{pv} along with i_{pv} stay at their corresponding values of MPP without getting affected from variations in irradiance level or load, where i_b is getting adjusted to keep at MPPT mode of operation.

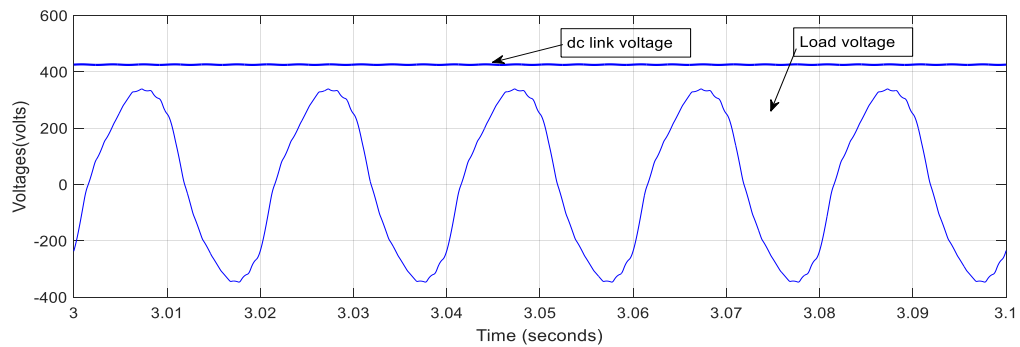


Fig. 21. Waveforms of v_{dc} and load voltage of the system for changes in load and irradiance level during MPPT mode under steady-state operation in MPPT mode.

The voltage of load and dc-link, V_{dc} are displayed in Fig. 20. Response of system under steady state when in MPPT mode of operation is displayed in Fig. 21. Voltage of load is 230 V rms and voltage of dc link are displayed in Fig. 21.

5.2. Under changes in load and irradiance level during mode change between MPPT & Non MPPT.

Table III: Parameters with which simulation is performed for changes in load and irradiance level during mode change between MPPT & Non MPPT.

Time(in seconds)	Irradiance Levels(KW/m ²)	Load Demand(watts)
0-1.2	0.75	450
1.2-2.2	0.75	250
2.2-3.3	0.75	300
3.3-4.2	0.75	250
From 4.2	0.75	450

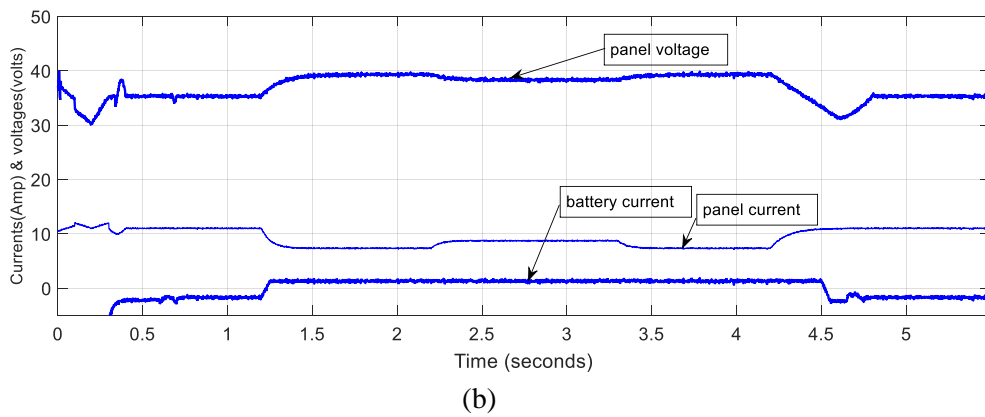
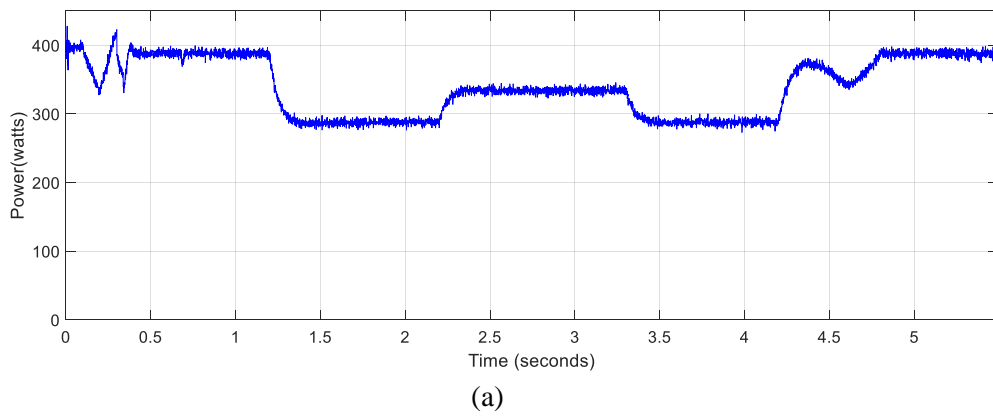


Fig. 22. Waveforms of P_{pv} , V_{pv} , i_{pv} and i_b of the system for changes in load and irradiance level during mode change between MPPT & Non MPPT.

Simulated waveforms of system when there is a transition between MPPT mode and non MPPT mode under variations in load demand are shown in Fig. 22 & Fig. 23. In the beginning, irradiance level is set as 0.75 kW/m² ($V_{mpp} = 35.4$ V, $I_{mpp} = 11$ A,) and load

demand was also set as 450 watts that is greater than P_{mpp} . As a consequence, system will operate in MPPT mode of operation through battery getting discharged. We can take of it by observing in fig. 22 (a) that PV power is less than load demand till 1.2 seconds, so battery is getting discharged to feed that deficiency. Load demand is decreased to 250 watts at 1.2 seconds where P_{mpp} is more than that load demand. So, the extra power of PV aids in battery charging. The instant current through battery reaches certain limit, system starts operating in non MPPT mode. Here when the load demand is 250W, PV is supplying 294W, so the balance power is charging battery.

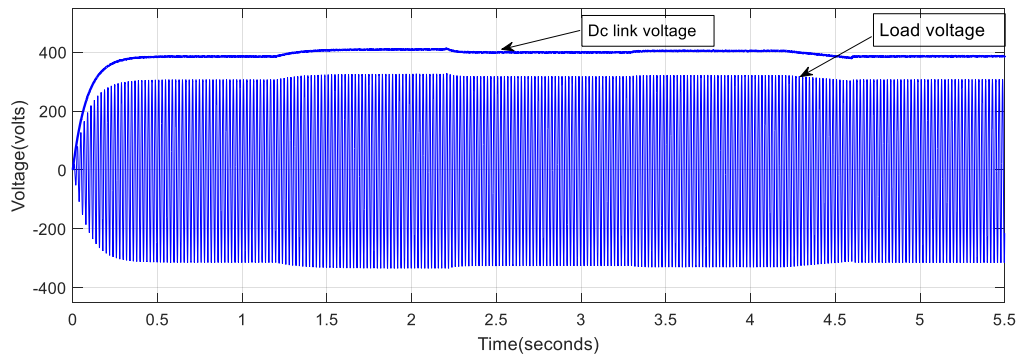


Fig. 23. Waveforms of v_{dc} and load voltage of the system for changes in load and irradiance level during mode change between MPPT & Non MPPT.

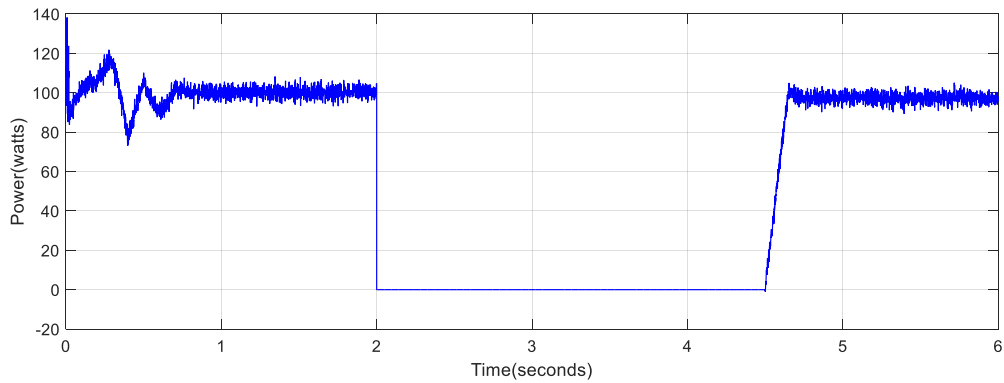
From fig. 22 we can infer that when system is operating in non MPPT mode, the PV panel operating voltage goes to right of the MPP i.e., more than V_{mpp} . At 2.2 seconds, load demand is enhanced to 300 watts. To feed this increase in demand of power, panel operating voltage comes a bit left side but still less than V_{mpp} i.e., on right side of MPP. When load demand is 300W, PV is supplying around 340W, this extra power charges battery. Load demand is again decreased to 250 Watts at 3.3 seconds, and operating point of PV panel again moves to right of MPP. Again when load demand is increased to 450 watts at 4.2 seconds, the operating point of panel reaches MPP to meet the load demand and discharging of battery also takes place to meet load demand. From 4.2 seconds, when load demand is 450W which cannot be supplied by panel alone, is getting delivered by battery. Thus we have noted that again system is operating in MPPT mode.

From Fig. 23 we can infer that V_{dc} varies whenever V_{pv} varies according to (9). But, Dc link voltage, V_{dc} stays in prescribed ambit of 350 to 460 V, resulting in conveniently maintaining load voltage around 230 V rms.

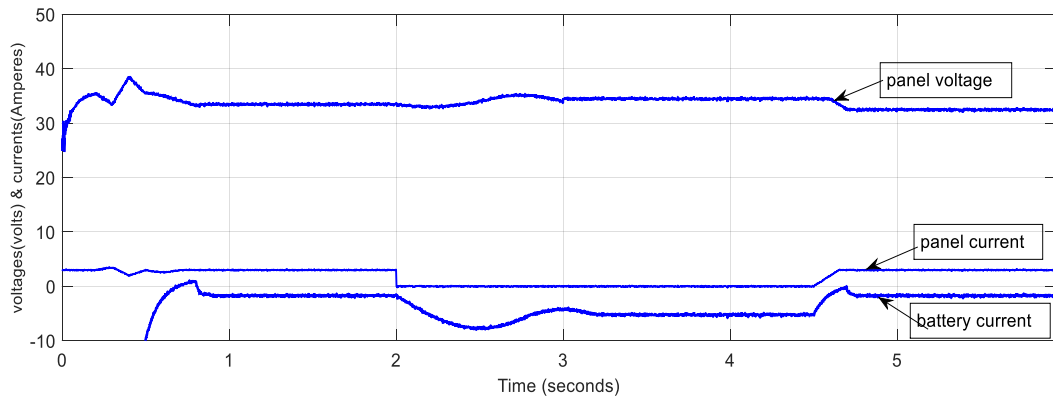
5.3.Under changes in irradiance level during mode change between MPPT & Battery mode.

Table IV: Parameters with which simulation is performed for changes in irradiance level during mode change between MPPT & Battery mode.

Time(in seconds)	Irradiance Levels(KW/m^2)	Load Demand(watts)
0-2	0.2	150
2-4.5	0	150
From 4.5	0.2	150



(a)



(b)

Fig. 24. Waveforms of P_{pv} , V_{pv} , i_{pv} , and i_b of the system for changes in irradiance level during mode change between MPPT & Battery mode.

The waveforms of simulation of entire system when there is a mode transition between MPPT mode and BO mode with variations in irradiance level are shown in Fig. 24 & Fig. 25. Initially load demand was set at 150 watts and irradiance value was at $0.2 \text{ kW}/\text{m}^2$ ($V_{mpp} = 33 \text{ V}$, $I_{mpp} = 3 \text{ A}$). This conditions were till 2 seconds. Till 2 seconds, load demand 150W, is delivered together by Panel and battery on load sharing phenomenon.

Irradiance is made zero at 2 seconds which leads to current through panel zero and the entire demand on load side has to be fed with battery, so it is called BO mode.

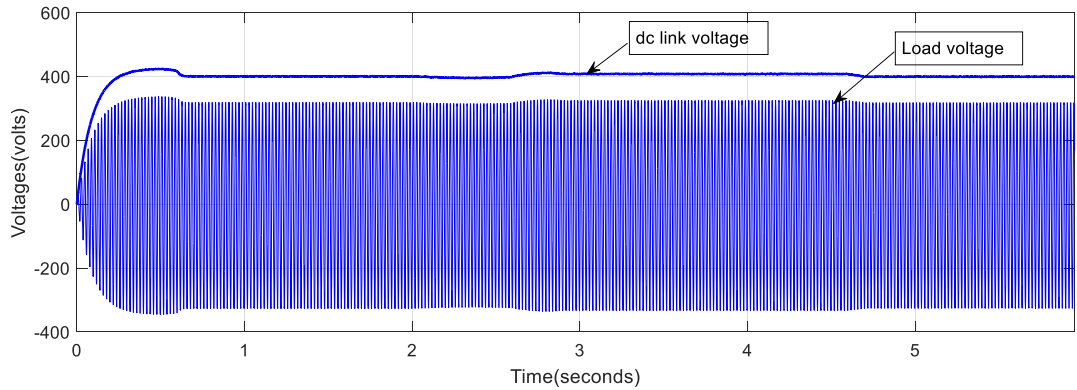


Fig. 25. Waveforms of v_{dc} and load voltage of the system for changes in irradiance level during mode change between MPPT & Battery mode.

Irradiance is reverted to 0.2 kW/m^2 at 4.5 seconds, so again from this instant, load demand will be met on load sharing phenomenon by both battery and PV panel. From Fig. 24 we can infer that voltage of PV panel is at its MPP value when system is The load voltage and dc link voltage, V_{dc} are displayed in Fig. 25.

Chapter 6

Conclusions and Scope for the future work

A stand-alone solar PV system specifically to employ in remote locations is discussed in this thesis. It is realized by incorporating a new topology TCDIC connected to a normal full bridge inverter to convert dc into ac. Major or important characteristics of this topology are:

- 1) The extraction of Maximum Power from PV panel, battery charge control, and dc voltage boosting are achieved by just one converter.
- 2) Need of exclusive converter for obtaining operation of PV panel at MPP is gone, there by resulting in optimized usage of converters of power.
- 3) improvement in efficiency of charging of battery as a single converter is there in charging path of battery
- 4) lesser count of components because only two conversion of power stages are needed.
- 5) The load and Input sources are isolated.
- 6) Lucid and efficient control structure guarantying suitable selection of operating modes and smooth transition among different possible operating modes.

Efficacy of this topology is consolidated through simulation. As a future work this topology can be integrated to grid with either single phase topology or three phase topology and can examine the performance of this topology under voltage fluctuations, partial shading, etc.

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